Designing 100BASE-TX Systems with the QFEX Family

AMD

Application Note

This application note provides a design reference for customers wishing to implement 100BASE-TX systems, using QFEXr™ for the PHY hardware. An overview of QFEXr is included, but for further detailed information, refer to the individual QFEXr data sheets. Although system design details such as interfacing QFEXr to repeaters and proper board design and layout with QFEXr are provided, only a few general high-speed design and general layout rules are addressed. Other sources of information for PHY layout and high-speed designs are listed in the References section.

INTRODUCTION

In response to the need for higher bandwidth than that provided by 10BASE-T, the IEEE committee defined a 100-Mbps standard (100BASE-X), borrowing PHY technology from the existing FDDI standard. This 100-Mbps standard, also known as Fast Ethernet, offered a 10-times greater speed using twisted pair (100BASE-TX) and fiber (100BASE-FX) for almost equivalent cost to 10BASE-T.

100BASE-TX defines transmission of data over UTP Category 5 cable and defines layers of functionality implemented to support 100-Mbps communication. A layer of particular interest is the physical (PHY) layer which defines the technology required to convert line signals into frames of data that other layers beyond the PHY layer can use. The PHY layer connects to hardware such as network cards, switches, and repeaters. This application note will focus on repeaters and PHY connectivity.

AMD recently introduced the first member of its PHY family, the QFEXr device. The QFEXr device is a four-port physical layer device used for 100BASE-X repeater applications.

100BASE-TX REPEATERS

Designing 100BASE-TX repeaters is similar to designing 10BASE-T repeaters over the same twisted pair interface. The differences in designing 100BASE-TX vs. 10BASE-T repeaters are a 10 times jump in data rates from 10 Mbps to 100 Mbps, the method of data decoding/encoding, and the availability of a Signal Detect function for link integrity. These features make 100BASE-TX more intricate than 10BASE-T, but 100BASE-TX repeater designs can provide benefits of higher data bandwidth for significantly less than 10 times cost.

As shown in Figure 1, a repeater and a PHY layer are needed to realize a 100BASE-TX repeater design.

Figure 1 shows the components of a 100BASE-T repeater. Note that the repeater is part of the Physical layer of the OSI model. To convert this into a 100BASE-TX system, the Medium and Medium Dependent Interface (MDI)become a twisted pair interface.

The PHY is comprised of three to four sublayers: the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Physical Medium Dependent (PMD), and, optionally, the Auto-Negotiation sublayer.

Note: *The Auto-Negotiation sublayer is not required in the 100 Mbps-only repeater designs.*

Although the PHY can seamlessly attach to the repeater, as shown in Figure 1, this is not the case with current market implementations, where only separate PHY and repeater devices are available. Therefore, an interface is required to connect the PHY to the repeater, and the most commonly used interface is the Medium Independent Interface (MII). The MII is also defined by the 100BASE-X standard and provides a level of compatibility between all silicon solutions today. An MII interface and its relation to the PHY is shown in Figure 2.

Using the MII allows an easy connection of any repeater with the MII interface to any PHY or other silicon device that also has an MII interface.

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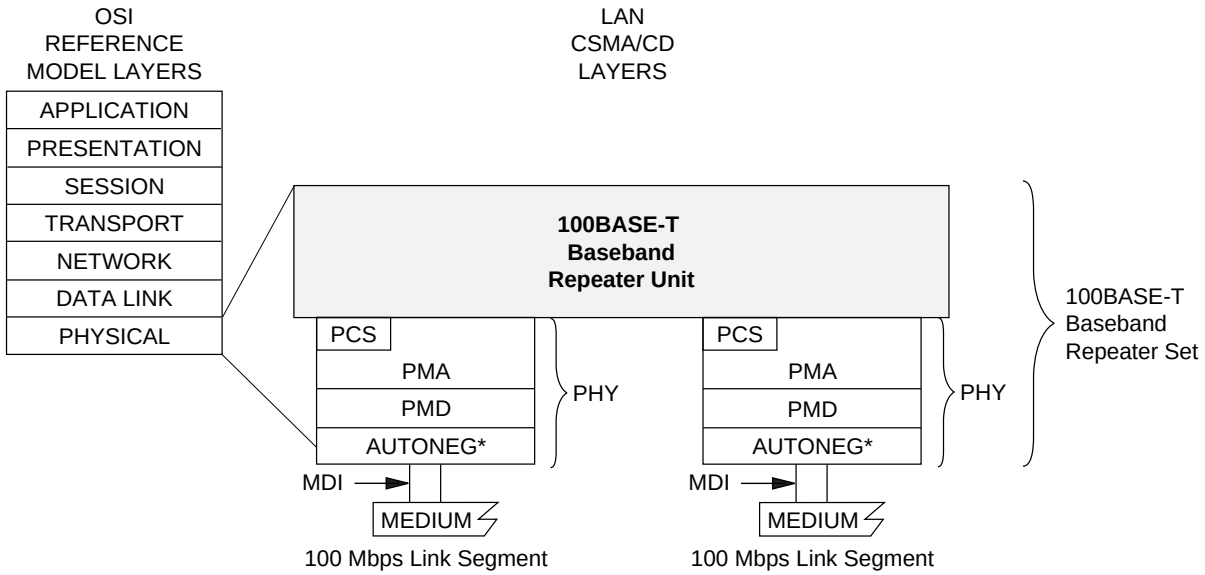

MDI = Medium Dependent Interface

PCS = Physical Coding Sublayer

PMA = Physical Medium Attachment

PHY = Physical Layer Device

PMD = Physical Medium Dependent

*AUTONEG not required for 100BASE-TX only.

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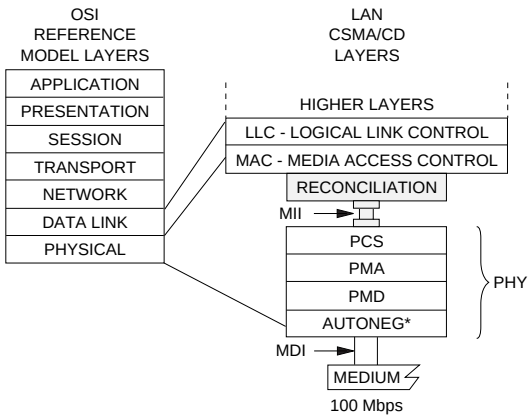
Figure 1. Repeater and PHY layers



MDI = Medium Dependent Interface
MII = Media Independent Interface
PCS = Physical Coding Sublayer
PMA = Physical Medium Attachment
PHY = Physical Layer Device
PMD = Physical Medium Dependent

*AUTONEG not required for 100BASE-TX only.

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Figure 2. MII interface

QFEX Family

The QFEXr device is AMD's silicon solution to address the PHY layer for 100BASE-X applications. The QFEXr device is a CMOS device that implements the PCS and PMA layers for four 100BASE-X ports, as shown in Figure 3.

The QFEXr device also offers the following features:

- — Programmable Carrier Integrity Monitor (CIM) for False Carrier event handling
- — Quad integrated Digital CMOS 100-Mbps clock recovery circuit
- — Optional scrambler/descrambler functions
- — Programmable Loopback modes
- — Programmable LED support
- — Far End Fault support
- — TX or FX support

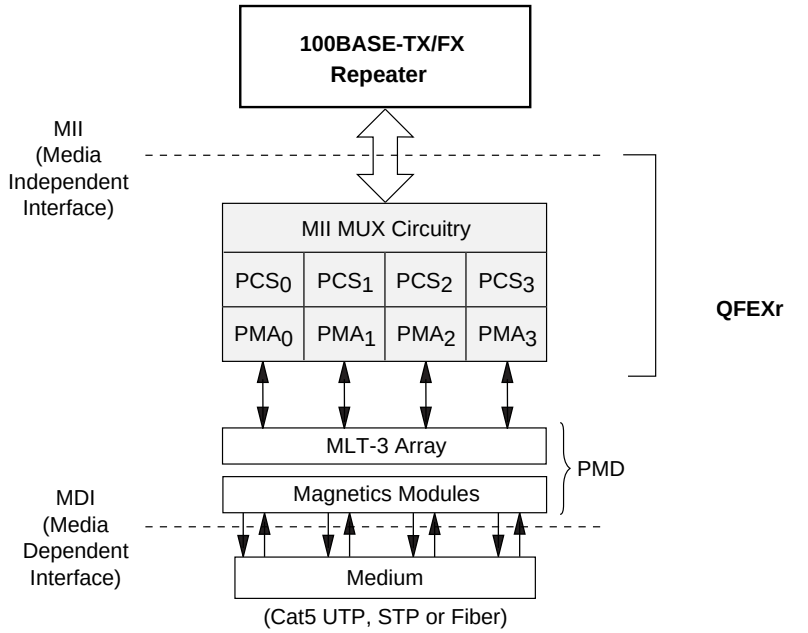

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Figure 3. Repeater, MII/PCS/PMA (outlined by QFEXr), PMD, MDI layers for 4 ports

The QFEXr device does not offer a PMD layer, but AMD has a relationship with Pulse Engineering to provide the necessary MLT-3 and magnetics support for twisted pair interfacing. The QFEXr device is available in a 100-pin version.

MII and Repeater Interface

There are two ways to interface a repeater or MAC to a PHY device. The standard way is using the MII interface, described in the 100BASE-X standard. The other method is using the standard 5-bit symbol interface, which will be described shortly.

The MII interface provides the basic signals needed to perform the necessary handshaking for the repeater and PHY to link and transfer data. Eighteen signals control the receive, transmit, and management processes. The 100BASE-X Reconciliation layer then converts these signals into primitive directives (data request and indication, carrier indication, and signal indication) that inform the PHY of what's happening across the interface.

The QFEXr device offers a Shared MII port. In repeaters, data is received on one port and is broadcast through the other ports. Pin count is greatly reduced, as seen in the 100-pin QFEXr package.

With this Shared MII, connecting four PHY ports to the repeater is much simpler than connecting four separate MII ports. The connection to the repeater through the MII port requires no glue logic, except for passives required for AC termination and reduction of high-speed effects.

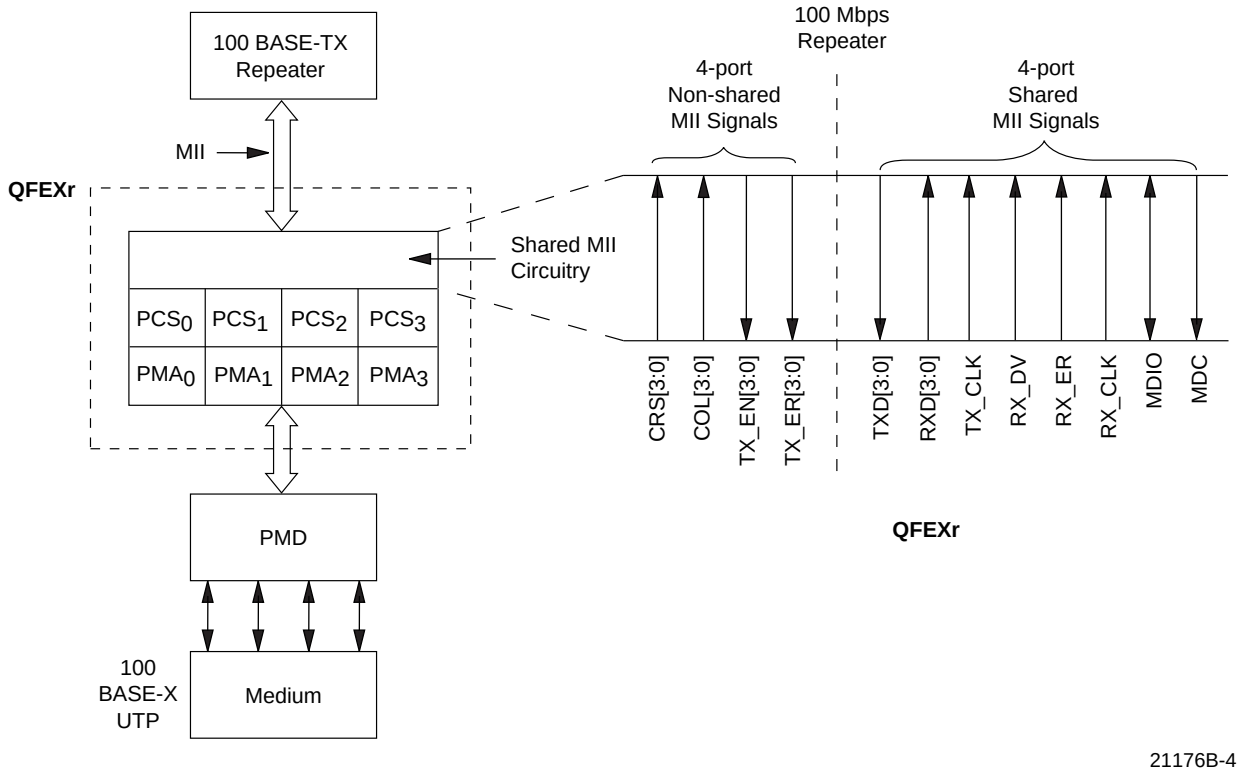


Figure 4. QFEXr Connection to Repeater (using Shared MII Interface)

As seen in Figure 4, the connection to the repeater through the MII port requires no glue logic, except for passives required for AC termination and reduction of high-speed effects.

For transmitting, the TXD[3:0] bus is connected directly to the repeater, as are the transmit enable signals, TX_EN[3:0]. The QFEXr device provides the option for using TX_CLK or system CLK as the internal timing reference. So, TX_CLK may or may not be used. TX_ER from the repeater is tied to all four TX_ER signals on the QFEXr device to inform all ports of any possible transmission error.

When receiving, the RXD[3:0] bus is connected directly to the repeater, and the ENRCV[3:0] (port receive

enable) signals are connected to RXE inputs on the repeater. RX_DV, RX_CLK and RX_ER all connect directly to the repeater.

Note: *Buffering may be needed for bussed signals if implementing four independent MII ports, and clock synchronization may be required to drive the four RX_CLK signals to ensure minimal clock skew.*

Finally, CRS and COL lines connect directly to the repeater, as well as the management lines (MDC and MDIO). Buffering is also recommended for driving multiple management lines if using the four independent MII port mode.

Application Example: Interfacing to NSC 100RIC

To demonstrate the benefits of the shared MII interface, the following text explains how to design a repeater using the QFEXr device. The repeater used is National Semiconductor's 100RIC (DP83850), a 12-port repeater.

This sample design requires three QFEXr devices to be connected to the 100RIC's MII port. Figure 5 shows the logical connection between the QFEXr devices and the 100RIC.

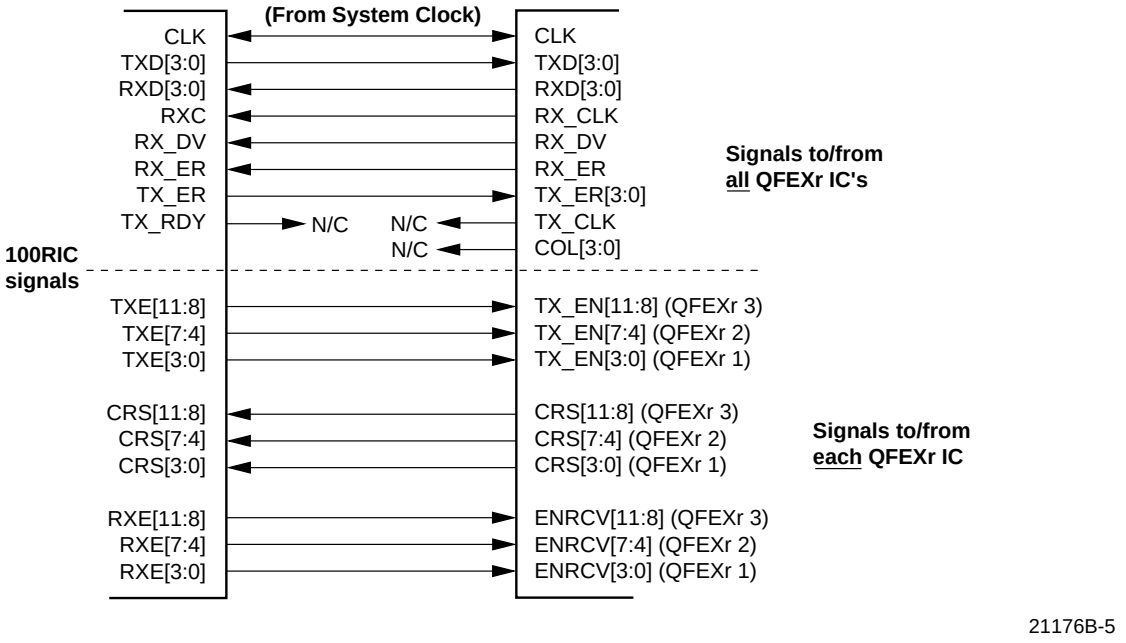


Figure 5. Sample Application: Multiple QFEXr Connections to NSC 100RIC

A 12-port repeater is a straightforward design using three QFEXr devices and the 100RIC. There is no extra logic required, except for optional buffers which can be used to ensure drive capability in all circumstances. For ease of display, the signals are separated into two types: those signals to/from all QFEXr devices, and those to/from each QFEXr device.

Common signals from the 100RIC to all QFEXr devices are TXD[3:0], RXD[3:0], CLK, RX_CLK, RX_DV, RX_ER and TX_ER. Thus, each QFEXr device receives that group of signals from the 100RIC. Some 100RIC outputs will drive multiple inputs, such as TX_ER, which will connect to 12 QFEXr TX_ER signals. It is possible to drive these inputs without buffers. Also, some 100RIC inputs will receive multiple QFEXr outputs, such as RXD[3:0], RX_CLK and RX_DV in a multiple QFEXr system. However, there is limited cause for concern regarding fanout, since only one port and, therefore, only one QFEXr device will be transmitting to the 100RIC at any one time. In the event of a collision (one port transmits while another receives simultaneously), the PHY (QFEXr) will notify the 100RIC with a JAM sequence (repeated out to all ports), but still only one QFEXr device will be using the bus at any one time. In this example, the system clock is used instead of TX_CLK. The 100RIC does not have collision indication inputs and cannot support COL[3:0]. Both LCK (100RIC) and the three CLK (QFEXr) signals are driven by a buffered system clock.

Signals to each QFEXr device means that those respective signals are mapped 1:1 on each device. So, 100RIC TXE[7:4] signals are mapped directly to the QFEXr device 2 signals TX_EN[3:0], or in the system, to logical signals TX_EN[7:4]. CRS signals map directly from QFEXr devices to the 100RIC. The QFEXr ENRCV signals are not directly part of the MII standard interface in the 100BASE-X standard, but connect directly to the 100RIC's RXE signals. It is possible to add buffers to increase the drive of each pin, but it is not required.

As a final note, it is highly recommended to provide AC termination on most signal lines. If a signal fans out to multiple devices, each trace should be terminated accordingly.

Driving Multiple PHY's

Buffers may be needed to create large unmanaged repeaters using the QFEXr device. In a sample 12-port design, three QFEXr devices can share common signals without significant drive degradation, but to provide additional drive capability, reasonably fast buffers should be used.

PCS

The PCS lies below the MII interface. It is in charge of the following functions in 100BASE-X:

— Encoding and decoding MII data nibbles to and from 5-bit code groups. This is accomplished by using the 4B/5B algorithms.

— Generating Carrier Sense and Collision Detection indications.

— Serialization and deserialization of code groups for transmission and reception on the underlying PMA layer.

— Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA layer.

The QFEXr device implements the PCS layer per the 100BASE-X standard and also add a scrambler/descrambler block to complete the PCS functions, as shown in Figures 6 and 7.

On receipt of data, after it has passed through the PMA layer (clock recovery, see below), the serial data is deserialized and passed on as a 5-bit entity to the descrambler block. Scrambling and descrambling is offered on the QFEXr device as a means of reducing EMI peaks in the radiated signal (data) caused by repetitive patterns of 0's and 1's. Scrambling is done by adding the output of a random number generator to the data signal. The descrambler does the reverse process for received data. The scrambler/descrambler function can be set to minimize emissions as needed on the QFEXr device.

Following the descrambler block, received data is aligned and decoded. Encoding and decoding is performed using the 4B/5B code-group algorithms. Decoding 5-bit PCS code groups into 4-bit MII groups effectively reduces the 125-Mbps physical channel rate to a 100-Mbps physical layer interface. The reverse happens for transmission. Here, JK and TR delimiter pairs are added (for transmission) or removed (for receive) from the packet when the data packet is aligned. Refer to the 100BASE-X standard or the QFEXr data sheet for the code-group mapping tables.

Once the data is decoded and converted into 4-bit nibbles, it is passed on to the MII interface on RXD[3:0] to the repeater. All other MII signals, such as RX_ER and RX_DV, are set appropriately.

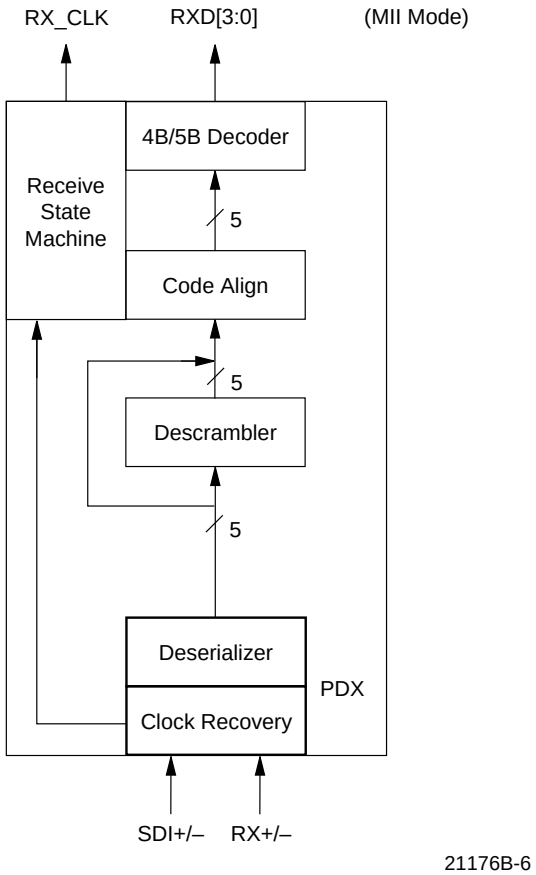


Figure 6. QFEXr Receive Path

Figure 7 illustrates the transmission process through the QFEXr device from the MII. Data is received on TXD[3:0], encoded into 5-bit PCS code groups,

aligned, scrambled (if necessary), and serialized for the PMA layer.

Loopback modes within the PCS block are available in the QFEXr device as follows:

— From MII {TX_ER, TXD[3:0]} to {RX_ER, RXD[3:0]

— From the 4B/5B encoder output to the 5B/4B decoder input (after code alignment)

— From the scrambler output to the descrambler input

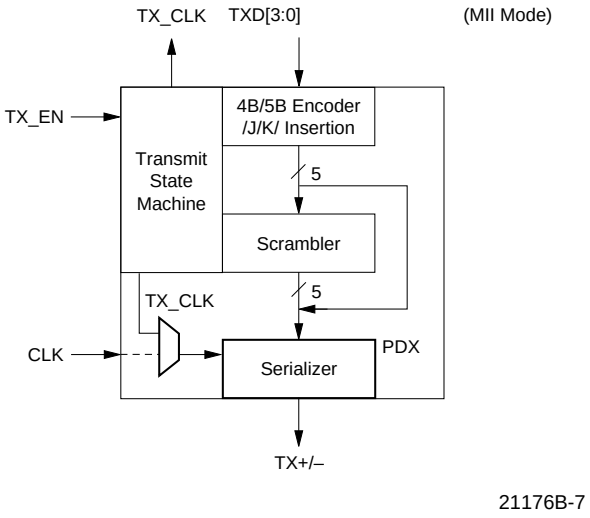


Figure 7. QFEXr Transmit Path

PMA

The PMA layer lies below the PCS interface. It is in charge of the following functions in 100BASE-X:

— Clock recovery from the NRZI data provided by the PMD

— Mapping of transmit and receive code-bits between the PMA's client and the PMD

— Optionally, generating indication of carrier activity and carrier errors from the PMD

— Optionally, sensing receive channel failures, and detecting and transmitting the Far End Fault Indication (FEFI)

The QFEXr device uses an all digital CMOS core for clock recovery called the Physical Data Transceiver (PDX).

In transmit, after passing through the PCS, the 5-bit symbol is clocked into the PDX, serialized, converted to NRZI format, and shifted to the TX± outputs at PECL-compatible signal levels. The PDX uses system CLK as the frequency and phase reference to generate the serial link data rate. Thus, the PDX requires a continuous external reference that it can derive its internal clock from, which is multiplied by 5 to generate the 125 Mbps channel rate. The external reference clock must meet 100BASE-X frequency and stability requirements (±50 ppm).

When receiving, data coming into the RX± inputs is streamed into the PDX, which recovers the clock and then uses the clock to recover the data. The data, in an unframed 5-bit symbol, is then sent up to the PCS level for further operations. The PDX is capable of recovering data correctly within ±1000 ppm of the 25 MHz clock signal.

Carrier Detect, Link Monitor, and Far End Fault Detect and Generate functions are also provided by the QFEXr device. Refer to the 100BASE-X standard for details on these functions.

Loopback modes within the PMA block are available in the QFEXr device as follows:

— From the 5-bit data output to the 5-bit data input inside the PDX block

— From the PDX serial output to the PDX serial input

Carrier Integrity Monitor

To protect the repeater from spurious fault conditions as well as preserve communications, the 100BASE-X standard has included features that should be implemented in the various PHY layers, including FEFI, link monitor, and CIM. Fault conditions can be caused by faulty wiring and disconnected/connected wires.

The CIM is specified as a feature the repeater provides (Clause 27). The CIM detects certain faults like the False Carrier and informs the repeater. A False Carrier is an indication of activity on the line, but is not a valid packet of data (any carrier event that does not begin with a valid start of stream delimiter). The repeater will issue a Jam sequence (a series of 3s and 4s in hexadecimal) to all ports (except the receiver) and to the MII to inform the ports of the false carrier and that nothing should be received until the false carrier ends, or the false carrier timer times out. If a successive false carrier signal follows, the receiving port is partitioned.

The CIM is part of the PMA interface and is the responsibility of the repeater PMA to count false carrier events and implement the necessary requirements per the 100BASE-X repeater section of the standard.

Many 100-Mbps repeater devices available today lack the CIM feature, and it has fallen on the part of the PHY device vendors to provide an interim solution. The QFEXr device offers a full CIM feature for repeaters

without CIM capability. The CIM function is implemented on a per port basis and can be turned off if the repeater has its own CIM function.

PMD

The PMD sublayer lies below the PMA and was originally derived from the FDDI standard. Thus, it has been defined to support 125-Mbps fiber and shielded and unshielded twisted pair media. The PMD basically translates the NRZI-coded data to and from signals suitable for the specified medium, which is in this case twisted pair. 100BASE-TX data must be transmitted using at least Category 5 UTP. The QFEXr device can transmit data to MLT-3 and fiberoptic transceivers over the TX±, RX±, and SDI± pins.

MLT-3 Transmission

For twisted pair, data translation is accomplished most often by using MLT-3 (Multilevel Transmission - 3 Level). MLT-3 is very similar to NRZI, except that it adds a third level of voltage to represent the data. Thus, where NRZI data falls between 0V and a predetermined limit of V, MLT-3 data can be any of 3 levels: 0, +V and -V. MLT-3 uses a fundamental frequency one-half that of NRZI. With that, MLT-3 achieves data transmission at the same data rate but with lower spectral energy (e.g., lower EMI emissions) than NRZI. Often, MLT-3 is further combined with scrambling to eliminate repetitive patterns in the data that causes more peaks in the EMI spectrum.

When designing for MLT-3, the following several considerations must be attended to, due to the type of media being used:

— Adaptive Equalization

— Baseline restoration

— Transmit Conditioning

Adaptive equalization is a key feature in MLT-3. Data transmitted over twisted pair wire can suffer much attenuation (signal loss) or experience varying amounts of attenuation, due to different frequency components of the signal itself, as well as cable length. When the signal is received, the device has to reconstruct the original signal and somehow overcome this loss. Adaptive equalization enables the MLT-3 device to compensate for this loss and for varying cable lengths by analyzing the incoming signal and adjusting the equalizer accordingly.

Baseline restoration is another key feature required for MLT-3. A problem with data transmission is baseline wander, which is described as DC drifts in the incoming signal baseline wander that may occur due to data pattern dependent DC shifts and the inherent low frequency bandwidth of the channel and AC coupling transformers. If not corrected, the droop component of the transformers dominates and “drags” the signal amplitude down below baseline so as to cause data errors or link failure. Baseline restoration circuitry compensates for this wander by comparing the incoming signal with a reconstructed reference. The difference is filtered and used to affect low frequency compensation in order to maintain the equalized signal at the reference level.

Transmit conditioning includes providing the correct transmit amplitude at the TX outputs, as well as generating output waveforms synchronized in timing with minimal jitter effects.

Figure 8 shows the QFEXr connection to MLT-3 and magnetics components for 100BASE-TX applications.

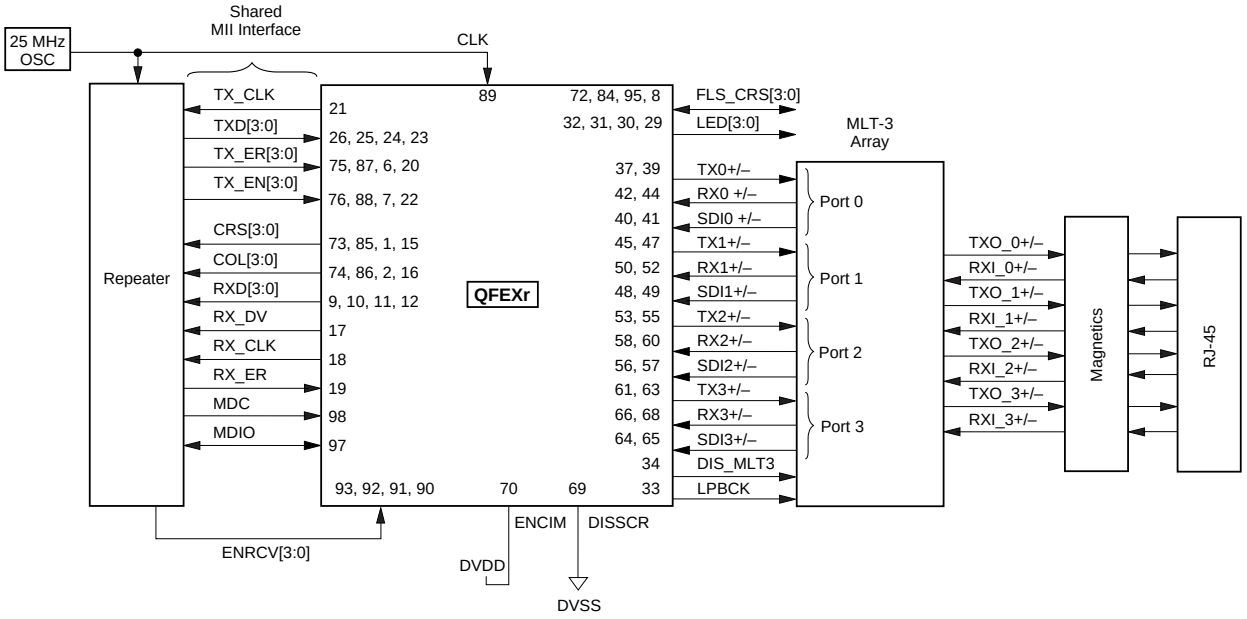
The QFEXr device has a DIS_MLT3 pin that can be used to enable the MLT-3 interface whether needed or not. Although the QFEXr device does not implement MLT-3, AMD has an alliance with Pulse Engineering to provide MLT-3 support for the QFEXr device. Refer to the *References* section for more information. Other MLT-3 vendors include National Semiconductor, Micro Linear, and GEC Plessey.

PMD Magnetics

As in 10BASE-T, magnetics solutions are still needed to provide isolation between the cable and the PHY layer. Available magnetics modules also support FDDI, ATM, and 100BASE-TX over unshielded (UTP Category 5) and shielded twisted pair (STP). The modules are mainly used to provide isolation for data transmission from the cables. Most modules are comprised of any combination of filters, transformers, and chokes for common mode rejection, but filters and chokes are optional and can be obtained separately. They provide high voltage isolation (ESD protection @ 2 KV), wide bandwidth, and fast rise times.

An important point to note is to follow termination guidelines as recommended by the magnetics manufacturer. This is interpreted as a combination of resistors and decoupling capacitors and proper grounding on non-data lines (including centertaps) used to reduce common mode noise, that provides significant reduction in EMI and noise susceptibility. Center tap connections can typically provide a 10 dB improvement in common mode rejection. Often, the magnetics module can be the savior for a 100-Mbps system to pass FCC tests, which is much more sensitive than a 10-Mbps system.

The magnetics modules connect to the RJ-45 interface and to the transceiver device through the RD-to-RX and TD-to-TX signals. Proper termination and impedance matching to MLT-3 devices is often provided in application notes of the transceiver vendor. Their guidelines need to be followed carefully to obtain the best performance from cable to PHY.



***Note**: Required pullup/pulldown resistors and MLT-3 details are not shown. Consult MLT-3 vendor for recommendations.*

Figure 8. QFEXr Connection to MLT-3 and Magnetics Components for 100BASE-TX

GENERAL CIRCUIT DESIGN AND LAYOUT GUIDELINES

High speed design is always a tricky issue, and it becomes critical to follow basic guidelines in order to ensure a clean design.

To optimize a design for the QFEXr device, designers must follow basic rules in layout and placement, decoupling and isolation, clock and oscillator considerations, general terminations, power supply filtering and plane partitioning, and finally, EMI considerations. The combination of these rules will contribute greatly to a proper functioning 100-Mbps repeater system. Above all, suggestions from PHY, transceiver and magnetics vendors should be followed when designing a specific solution.

Parts Recommendations

- Resistors should be 1% tolerance.
- Capacitors:
  - For low frequency and large value decoupling, use electrolytic capacitors.
  - For high frequency and small value decoupling, use X7R and C0G capacitors.
- Recommended ferrite beads are Fair Rite 274-3019-446.
- Fully Shielded RJ-45 8-position jacks.

Placement and Layout

Placement and layout are the key components of board design. Much care if given to performing these tasks properly ensures a good design. Noise, ringing, transmission lines, and other factors have to be controlled. Data lines should have a controlled impedance and be properly terminated, and power supply pins should be protected by proper filtering techniques. All PC traces should be treated as transmission lines with continuous ground or power planes beneath each trace.

Placement of the QFEXr PHY device should be symmetrical with respect to the repeater device. This will provide more equal trace length to each PHY and counteract most timing/skew problems, especially with synchronization of the clock to all clock-based components. The QFEXr devices should also be close to the repeater or buffers to minimize trace length and excessive line ringing, due to high-speed data transfers. Proper termination should be used.

When placing decoupling components, traces should be kept as short as possible, especially for the transceiver

interface. Short traces minimize noise interference. These components, if using many transceivers, should be placed symmetrically across the board to avoid uneven parasitic loading. It is preferred to have decoupling components on the same side as the device, to avoid routing via through different planes and having components on the solder side, as well as absorbing noise from different planes.

Other general guidelines for signal trace routing include the following:

- Only differential pair signals should be run parallel to each other, since they provide a canceling effect on noise. However, (non-differential) parallel traces tend to induce crosstalk. Differential signal traces should be as short and direct as possible.
- 90˚ trace corners should be minimized. Bevel them at a 45-degree angle or as appropriate (chamfered or radiused approach). Differential pairs will require equal trace length, even with 45-degree angle traces. Sharp edges add parasitic effects that translate into minute impedance mismatches. At high frequencies, additional charge accumulation causes an increase in capacitance at the corners of the trace bend, which results in a concentration of electric fields.
- Minimize the number of vias for any one given signal trace. It is recommended that the signal trace remain only on one plane (component or solder) or go directly into the power or ground layer (if it is a power/ground signal). As vias pass through layers, the impedance of the trace changes and it is difficult to maintain constant impedance after the via.
- Traces carrying large amounts of current should be thicker than normal signal traces. Otherwise, the traces may be easily burned out by current overloads.
- Maintain constant trace lengths to avoid impedance mismatch and reflections.
- Avoid long traces, as they generate and pick up radiated noise from around the board. They also tend to be a common source of crosstalk.

The system designer can add extra pads that are capacitor/resistor-sized so that components can be easily added during the debug stage. The same applies to IC's, where some 14/16/18-pin package pads can be placed on the board to accommodate any changes during the debug stage.

To reduce EMI emissions, the following rules should be observed for board layout:

- The PCB should be multi-layer (4 to 6 layers), with individual power and ground sublayers for best high frequency and EMI performance. Component traces can be run on the component and solder sides, but preferably only on the component side, unless it is absolutely critical to place decoupling components underneath devices. The power and ground layers should be in the inner layers of the PCB.
- Proper ground and power plane partitioning (see below) should be followed, as per recommendations from transceiver vendors.
- Use shielded components wherever possible. This refers to RJ-45 jacks, with contacts to chassis ground.
- Proper termination of components and unused (high speed) pairs in their common mode impedance (to chassis ground) to minimize cable reflections and common mode standing waves. Follow transceiver vendor recommendations.
- When adding spacers to elevate the system from the chassis, ensure that the screws are not placed symmetrically (either straight rows/columns or diagonals) throughout the board. The screws tend to act as antennas and create wave harmonics that will affect the EMI testing. Optionally, teflon screws can be used to support the board.

Clock/Oscillator Considerations

The clock is an equally important device in repeater design, since it is from the main clock that any reference clocks (TX_CLK, RX_CLK) are derived, and it is used for the various PLLs. With a noisy clock signal, PLLs (even QFEXr's digital PLL) will have difficulty locking onto the data packets.

Oscillators are recommended, in the metal can package, due to the shielding. They should be decoupled as recommended by manufacturer's guidelines.

Oscillators should be placed close to repeater and PHY components, or if not possible, they should be placed close to the repeater component, and same-length traces should be used to the QFEXr devices. Traces should be placed further away from other long traces.

General Rules On Termination

Termination of signals is a requirement in repeater design. Termination helps reduce ringing/cable reflections and impedance mismatching. A variety of termination networks are available, and manufacturer (PHY/QFEXr, transceiver/MLT-3 and magnetics) recommendations should be heeded.

AC termination is needed to minimize high-speed reflections. This can be accomplished by placing a resistor in series with a capacitor to digital ground. This is recommended on the following signals for the QFEXr device: RXD[3:0], TXD[3:0], RX_DV, RX_ER, TX_ER,

RX_CLK, and TX_CLK. The effect of the termination will also slow down any fast ramping CMOS signals.

Additionally, some QFEXr signals are pulled down with weak pulldown resistors to pull down those signals from a tristate level. RX_DV, RX_ER, and RX_CLK should be pulled down with 20-KΩ resistors.

Termination is also needed at the PECL level. Signal traces should be effective 50-Ω transmission lines and can be achieved using Thevenin termination or other recommended schemes from transceiver and magnetics vendors.

Most PHYs, including the QFEXr, provide differential Signal Detect (SD) pairs to the transceiver/MLT-3 devices. However, some MLT-3 devices do not offer differential SD pairs, and to counter this, designers should follow transceiver vendor termination guidelines, where the PHY SD signal is terminated with a different divider network.

The unused pairs of the RJ-45 jacks should also be terminated to improve EMI performance. This can be done in several ways, including 50-Ω resistors and RC networks. Consult magnetics vendor application notes.

Power Supply: Decoupling and Filtering

With a complicated high-speed design, noise can be picked up and propagated easily through the devices. If this noise is in the power supply lines, device and system performance is compromised.

DVDD signals should be decoupled as closely as possible to the IC. Ferrite beads can be used to isolate power planes (see the *Plane Partitioning and EMI Considerations section*), and an appropriate selection of capacitors can be placed around the board to filter out other frequencies. In general, 10-100 μF tantalum or electrolytic capacitors filter line frequencies and act as high speed filters. An additional ferrite bead can be used to help the effectiveness of the capacitor on the power input. 0.1 μF capacitors will help filter out higher harmonics (100 MHz and higher).

Other recommendations are as follows:

- 0.1 μF to 1.0 μF capacitors should be used for logic decoupling
- 0.01 μF to 0.1 μF capacitors should be used between each port's power/ground signals
- A large (10-30 μF) capacitor can be used between the power and ground planes at the sides of the IC package with many DVDD inputs

Use Table 1 to decouple the QFEXr power and ground signals.

Table 1. Decoupling Guidelines for QFEXr Devices

Signal Name	Function	Decoupling Capacitor Value	Notes
DVDD	Digital power supply	0.1 μF	Connect to DVSS through decoupling capacitor.
DVDD_D	PDX power supply	0.01 μF	Connect to DVSS_D through decoupling capacitor. Recommend connecting to DVDD through Ferrite Bead.
DVDD_Ex	PECL power supply	0.01 μF	Connect to DVSS_Ex through decoupling capacitor (x=0,1,2,3). Recommend connecting to DVDD through Ferrite Bead.
DVSS	Ground		Extra grounds connected to DVSS plane.

Plane Partitioning and EMI Considerations

100BASE-TX uses MLT-3 line coding (with a fundamental frequency of 32.5 MHz) to shift 90 percent of spectral energy to below 40 MHz. Without it, most systems, even with good system design, would not be able to pass standard EMI tests.

In general, digital areas should be partitioned from analog areas, which are extremely sensitive to noise. Digital signals alone suffer greatly since the fast switching times of digital components cause a significant amount of energy to be dumped into power and ground layers, generating significant overshoots and undershoots on the line. Any analog circuitry on the same plane will also experience the energy fluctuation, which can improperly bias the transistors, possibly causing the circuits to malfunction.

A lowpass filter combination of a ferrite bead (inductor) and capacitors provides a cleaner, filtered power plane for analog considerations. Ferrite beads are more effective than coils. At DC, the ferrite bead acts as a short, providing a low-resistance path for the power on the analog plane. The unwanted higher frequency AC noise sees the ferrites as inductors in a lowpass filter. Ferrite beads generally allow an increase in impedance as the frequency increases. Ferrite beads are quite useful as filters. However, be aware that they do add extra inductance to the plane and some added cost to the system. Therefore, they should be used sparingly and as needed.

Plane partitioning methods can vary widely from an ultra-conservative design (i.e., separate power and ground planes per port and PHY device, with DVDD filtering using ferrite beads) to the other extreme (i.e., large power and ground planes, with limited or no filtering). Because of the different components (noise sources, IC's, etc.) acting at the same time in the system, it is hard to pinpoint an exact design and layout method that will work in every case. Even the choice of components (transformers, etc.) can have an impact on the system passing FCC guidelines.

The recommendations listed here focus on the PHY and leaves it up to the designer to tackle the components and issues beyond the MII interface. Likewise, MLT-3 layout is dependent on the components and the MLT-3 vendor recommendations. Consult the MLT-3 transceiver vendor for information.

The QFEXr device is a four port device with MII interfaces and MLT-3 or PECL interfaces. The MII interface lies in the digital portion of the board and, therefore, should be overlaid by a digital power and ground plane. PECL ports can be overlaid by digital or PECL planes, but PECL planes are recommended. Notice that the QFEXr device should have a separate PDX plane to ensure a clean power signal is sent to the on-board PLL. Thus, layout for the QFEXr device should consider these three planes, as outlined by the following options:

Option 1

- Power plane layout:
  - — One PECL plane for each port, separated from main power by ferrite beads
  - — One PDX plane also separated by a ferrite bead
  - — Remainder of the device to reside in the CMOS VCC power plane with CMOS
- Ground plane layout:
  - — All ports and the device reside in CMOS VDD ground plane

Option 2

- Power plane layout same as option 1
- Ground plane layout:
  - — All ports reside in a separate PECL ground plane (no ferrite beads), separated from main
  - — Ground except in one area (the "neck")
  - — Remainder of the device to reside in CMOS VDD ground plane

Option 3

- Power plane layout same as option 1
- Ground plane layout:
  - — One PECL plane for each port, separated from main ground except in one area (the "neck")
  - — Remainder of the device to reside in CMOS VDD ground plane

An alternate power plane layout that seems to work is to provide one PECL plane for all ports and still maintain the separate plane for the PDX. A multiport design can benefit from this simplified layout, where each QFEXr device has its own PECL and PDX planes. However, it remains to be seen how the device can tolerate the added noise from inter-port crosstalk, as well as how stable the design would be to be able to pass FCC tests. This alternate scheme can be combined with any of the ground plane options listed above.

Figure 9 illustrates an example layout of power planes that aims to minimize potential noise sources which may detract from good EMI performance. It is important to separate the sensitive PECL from the noisy CMOS levels, and ferrite beads provide good filtering for this purpose. Having separate PECL planes also minimizes crosstalk from adjacent ports. Thus, four ferrite beads are recommended to separate PECL planes from the digital CMOS VCC plane. Additionally, to insure a clean power supply to the PDX, an additional ferrite bead is placed on the DVDD_D pin or on the plane underlying that pin to filter out noise from the connecting CMOS VCC plane. So, each QFEXr device can have up to five ferrite beads for power plane isolation. In multiport systems and using the alternate power plane layout option, this can be relaxed to two ferrite beads, one for the PECL plane and one for the PDX plane of the QFEXr device.

Layout of the ground plane will greatly affect the design, as foreseen by the above three options. Ground plane layout, as well as power plane layout, should take into consideration the signal-return path for the AC current generated every time a signal switches. Once the signal has returned, the current loop has been completed. AC return signals have an entire plane in which to choose a path, but they take the path of least impedance (inductance and capacitance) to the current and not necessarily in a straight line. If there are physical breaks in the return signal plane, the signal has to circumvent the break, thereby, increasing inductance and loop size.

The easiest ground plane layout as shown in the options would involve a common digital ground plane, connecting with the remainder of the system beyond the MII interface. However, because of the CMOS levels, a fair amount of noise can affect the PECL outputs. In light of this, a separate PECL ground plane would serve to separate most of the interference. The PECL ground plane and system ground plane would be two separate islands with a cut at the joining of both planes, placed appropriately to aid in the return signal path. This cut (or "neck") is the only "entrance" for ground into either plane, and a decoupling capacitor can be added to moderate the frequency behavior. Ferrite beads are

not recommended to isolate system ground from PECL ground, since ferrite beads add extra inductance that affects the return signal path. For further PECL port isolation, individual PECL ground planes can be added at the expense of a more intricate design to minimize signal path return. Separate PECL ground planes are also more tedious to lay out in multiport designs.

Each plane is separated by a ferrite bead (recommend Fair Rite 274-3019-446) that minimizes noise being conducted through to the next plane. Differential pair traces should be completely shrouded by the power/ground plane it is in and should not cross into other power/ground planes.

The plane area under the magnetics is left void for optimum noise separation between the transmit/receive and chassis planes. The chassis plane connects directly to the RJ-45 jacks, which are recommended to be fully shielded. Additionally, 2-K volt capacitors connected to chassis ground are required for ESD protection, per the 100BASE-X standard.

CONCLUSION

100BASE-TX repeater design is more intricate and requires a greater design effort than 10BASE-T design. However, there is a great amount of knowledge readily available to designers since high-speed design is already upon us.

The QFEXr device is relatively straightforward to design into a 100-Mbps repeater system. With integrated four-port capability, the reduction in board space and related components (otherwise needed for single port PHYs), the QFEXr device provide an easier and more cost-effective design for customers.

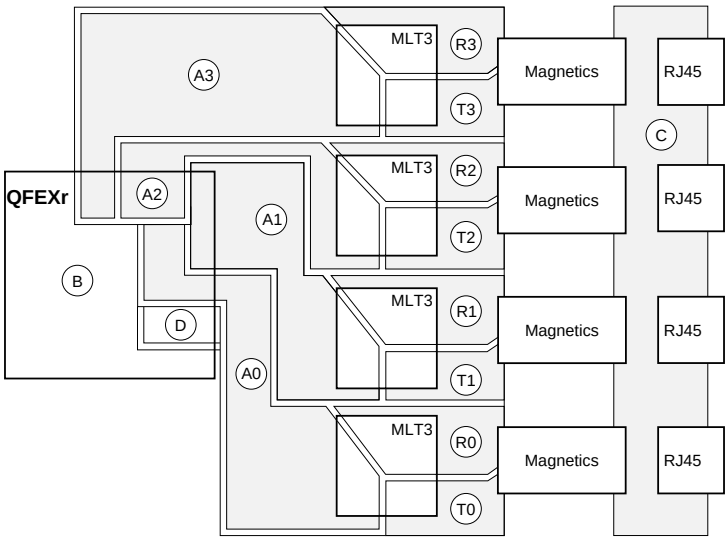
By following these rules for high-speed design and recommendations of repeater design with the QFEXr device, 100BASE-TX repeater designers should be able to make the transition from the 10 Mbps arena in a single leap.

Note 1:

The Analog Receive and Transmit planes shown here are sample recommendations by the MLT-3 transceiver vendor. Consult with the vendors regarding optimum system layout guidelines.

Note 2:

Ground planes need not be partitioned like power planes. Refer to the section "Plane Partitioning and EMI Considerations."



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Legend:

Group	Subgroup	Description
A	–	100 BASE-X PECL Plane
	A0	Port 0 PECL Plane
	A1	Port 1 PECL Plane
	A2	Port 2 PECL Plane
	A3	Port 3 PECL Plane
B	–	TTL/CMOS Signals
C	–	Chassis Plane
D	–	PDX Plane

Group	Subgroup	Description
R (Note 1)	R0	Port 0 Receive Plane
	R1	Port 1 Receive Plane
	R2	Port 2 Receive Plane
	R3	Port 3 Receive Plane
T (Note 1)	T0	Port 0 Transmit Plane
	T1	Port 1 Transmit Plane
	T2	Port 2 Transmit Plane
	T3	Port 3 Transmit Plane

Figure 9. Power Plane Partitioning (Note 2)

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