589D to 589E Technical Changes Addendum

3Com's 10Mbit LAN PC card 589X series, commonly known as Calvin PC cards, was revised from 589D to 589E in early 1999. This addendum documents hardware and software changes implemented to update the 589D to the 589E series.

MAC ASIC Changes:

One of the major changes made to Calvin was the development of a new media access controller (MAC) ASIC. Although the main core logic within the ASIC remained the same, some features were added, such as ACPI power management and the LED turn off capability.

The following registers were changed in the new MAC ASIC to support the ACPI function. All of the registers listed below are related to the ACPI power management functionality. The following tables show the windows and offsets indicating the locations of these addresses, as well as a brief definition of each register.

Window 7, Offset Ch:

Bit 6	LinkEvent (read only), link event occurred
Bit 5	MagicPktEvent (read only), magic packet occurred
Bit 4	WakeupPkEvent (read only), wakeup packet occurred
Bit 3	Reserved
Bit 2	PreLinkEventEn (read/write), enables link monitoring
Bit 1	PreMagicEvent (read/write), enables Magic Packet monitoring
Bit 0	PreWakeupEventEn (read/write), enables Wakeup Packet monitoring

Window 7, Offset 0h:

Bit 15	LanReqAttn (read only), can be access in ESR or Window 7, Offset 0h
Bit 9	ALanSigChange (read only), can be accessible in CSR or Window 7, Offset 0h
Bit 8	AlanReqAttnEn (read only), can be access in ESR or Window 7, Offset 0h
Bit 1:0	PowerState (read/write), D0, D1, D3

	D0 = 00 D1 = 01 D3 = 11

Extended Status Register (ESR), Offset 8h:

Bit 4	LanReqAttn (read/write), can be access in ESR or Window 7, Offset 0h
Bit 0	ALanReqAttnEn (read/write), can be access in SER or Window 7, Offset 0h

Configuration and Status Register (CSR), Offset 1h:

Bit 7	ALanChanged (read only), sets when there is weWakeup and aLanReqAttnEn enables
Bit 6	ALanSigChange (read/write), can be accessible in CSR or Window 7, Offset 0h. Asserts STSCHG# when aLanChanged and aLanSigChange setted

Note: To enable WakeOnLan, the following registers need to be set:

Window 7, Offset Ch = 07h	LinkEventEn, MagicEventEn, WakeupEventEn
Window 7, Offset 0h = 01h	D1
CSR [6] = 1	LanSigChg
ESR[0] = 1	LanReqAttnEn
To disable WakeOnLan: Window 7, Offset 0h = 00h	 D0

Window 4, Offset A

Bit 1	LEDDisable. (R/W) It disables the LED when set. When cleared the LED works normally.

The LED control bit in the 589E requires a change in the driver because the default mode is OFF (after power up or reset), unlike the functionality in the previous revision, the 589D. In the 589E, the LED will not be ON even if proper link is established unless the proper bit is set by the driver after initialization of the PC card.

Board Level Changes

Minor PCB changes were made to the 589E. When the 589E product was first launched, the PC card hardware remained almost the same, with the exception of the MAC ASIC. Since the new MAC ASIC did not radiate noise as in the previous ASIC, some filtering was removed from the board.

After the 589E product was released for production, a problem was reported to design engineering. Some laptops with the 589E PC card would lose network connection and, in some cases, would reset. The problems occurred only with new TI bridges such as the TI1220 and TI1250. After investigating the problem, it was determined that the root cause was a discrepancy in the timing of the IO16 latching between the TI bridges and 589E's MAC ASIC. In order to provide immediate and long term solutions for our customers, three corrective action items are currently being executed.

The first action item, implemented in February 1999, was to modify the driver to ignore the IO16 signal going to the host. The IO16 signal is generated by the MAC ASIC. In order to accomplish this task, the driver needs to modify two "I/O Control Register" bits in the PCMCIA/Cardbus bridges. The I/O Control Register controls the attributes of the two I/O windows. These registers should be set after initialization of the card. The following table describes the I/O Control Registers:

Bit	Description
7	I/O Window 1 Wait State
6	I/O Window 1 Zero Wait State
5	I/O Window 1 –IOCS16 Source, 1 = based on –IOIS16, 0 = based on I/O Window 1 Data Size bit
4	I/O Window 1 Data Size. 1 = 16 bit, 0 = 8 bit
3	I/O Window 0 Wait State
2	I/O window 0 Zero Wait State
1	I/O Window 0 –IOCS16 Source, 1 = based on –IOIS16, 0 = based on I/O Window 0 Data Size bit.
0	I/O Window 0 Data Size. 1 = 16 bit, 0 = 8 bit

The following bits need to be set by the 589E driver:

a) Assuming Windows 0 is the active window:

Write to offset 7, bit 0 → 1

bit 1 → 0

b) Assuming Window 1 is the active window:

Write to offset 7, bit 4 → 1

bit 5 → 0

These registers are part of the PCMCIA specifications and are expected to be present in all bridges. The drivers modified and loaded in the WEB are the NDIS3, NDIS4 and the ODI drivers. This is not a 100% solution and could show some performance degradation; nevertheless, it will prevent network connection loss or system reboots.

The second action item, implemented in March 1999, was to change the value of the pull-up resistor connected to the IO16 signal on the board. This change has proven to resolve the problem in more than 30 systems without affecting performance. Current products carry this change, with the exception of some products sold to a limited number of OEM customers. Although this solution has proven effective, 3Com's management believes that a third action item is required in order to guarantee total functionality for future TI bridges that may be implemented with yet different timing requirements.

The third pending solution, yet to be integrated, is a layout change. This change will pull-down the IO16 signal to a low at all times. The low value will indicate to the host that the PC card is capable of 16 bit accesses. This change does not violate the PCMCIA standard and it will be implemented in the July/August 1999 time frame.

EEPROM Content Changes

The differences between the 589D and 589E EEProm contents are listed below:

Word Offset	Description	589D	589E
.			
.			
06h	Product Code	4748h	4B51h
.			

0Eh	Compatibility Word	0002h	0003h
.			
14h	Adapter MajorRevision Level	0005h	C009h
.			
.			

Adapter MajorRevision Level word (14h)

LED control	[0:3]	To be set to 1001
Power saving mode	[14:15]	To be set to 11