EtherLink® 16 and EtherLink 16 TP Adapter Technical Reference Guide

Members of the EtherLink product family

For 3Com User Group Information
1-800-NET-3Com
or your local 3Com office

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3Com Corporation
5400 Bayfront Plaza
Santa Clara
California, USA
95052-8145

Manual revised by Jodi Schroeder. Edited by Anjali Puri. Technical illustrations and production by Tim Buckreus.

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Chapter 1
Introduction

This manual describes the EtherLink® 16 and EtherLink 16 TP adapter hardware architecture, configuration, and subsystem logic. The manual provides programming notes on creating a driver for the adapter by modifying an existing EtherLink/MC adapter driver. The information in this manual allows you to customize the adapter for the best performance in your network.

This manual is intended for use by experienced software engineers who write application or operating system software that either communicates with or resides on the adapter. The user must have a strong background in microcomputer systems.

Use this manual in conjunction with the *IBM® PC AT® Technical Reference*, the *Intel® 82586 Ethernet Controller Data Sheet*, and the *National Semiconductor® 93C06 EEPROM Data Sheet.*

For the EtherLink 16 TP adapter only, use this manual in conjunction with the *MicroLinear® BA116-006A Semi-custom Twisted-Pair Transceiver Data Sheet.*

The EtherLink 16 and EtherLink 16 TP adapters provide an 8- or 16-bit, high-performance network interface connection when installed in an IBM PC XT™, PC AT, or a Personal System/2® Model 25, 30, 35, or 40.

Throughout this manual, "the adapter" indicates both the EtherLink 16 and EtherLink 16 TP adapters, unless the adapter name is specified. Table 1-1 lists the features provided by the adapters.

Table 1-1. EtherLink 16 and EtherLink 16 TP Adapter Features

Both Adapters	EtherLink 16	EtherLink 16 TP
PC/XT form factor.	9.0 in. form factor.	9.4 in. form factor.
Self-sensing 8-bit XT bus or 16-bit AT bus interface.	On-board 10Base2 Ethernet transceiver and external AUI (DB-15) transceiver.	On-board 10BASE-T RJ45 transceiver.
64 KB of Zero Wait State (0WS) dual-ported RAM.	FCC Class B emissions certification (VDE Level B, TUV safety).	FCC Class B emissions requirements compliance.
10 MHz Intel 82586 Ethernet controller requirements.	Complies with UL safety. requirements.	
Socket for adapter boot ROM (8 KB, 16 KB, or 32 KB, depending on the revision level of the adapter).	External loopback testing option.	
Partial software compatibility with the EtherLink/MC adapter.		
Configuration saves to on-board EEPROM.		
Test mode pin presets adapter configuration at system startup.		

References

Throughout this manual, numbers are in decimal unless suffixed with an "h." For example

10h = 16
0FFh = 255

Chapter 2
Hardware Architecture, Configuration Logic, and State-Based Operation

This chapter provides an overview of the adapter's hardware architecture and configuration logic, and describes the adapter's operating states.

Figure 2-1 shows an adapter's hardware architecture.

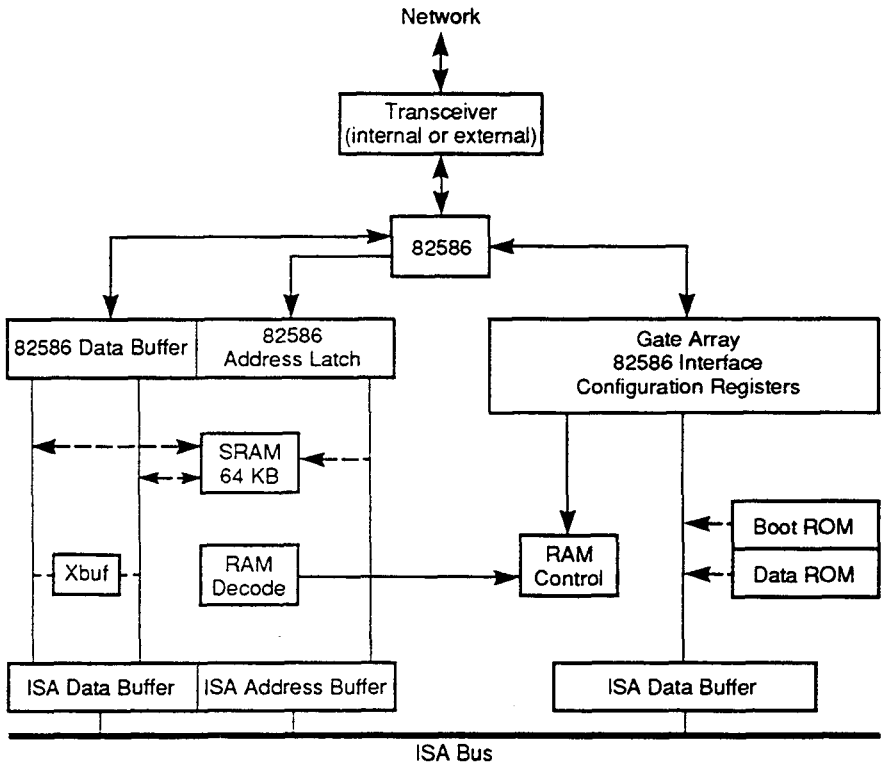

Figure 2-1. Hardware Architecture

See Chapter 3 for specific information about the adapter's subsystem logic.

Adapter Configuration Logic

The adapter allows you to set the following software configuration parameters:

- I/O base address
- ROM window base address
- ROM window size
- RAM window base address
- RAM window size
- Transceiver type selection (EtherLink 16 only)
- Zero Wait State (0WS)
- Data Mode

The values for these parameters are set using either the adapter's configuration utility on the *EtherDisk* diskette (sent with the adapter) or by programming the parameters directly into the adapter's EEPROM from the host computer using the I/O ports. See Chapter 3 for more information.

The IDSM and the Adapter's Operating States

The state-based operation of the adapter is controlled by the ID state machine (the IDSM) within the adapter's gate array. The IDSM transitions the adapter from one state of operation to the next, and is clocked by write operations that are issued to the ID port located at the fixed address 100h in the I/O address space of the host computer.

For example, the last state of operation of the IDSM, the RUN state, enables all of the adapter's functions. To operate in the RUN state, the IDSM sequences through each preliminary state of operation in the following order:

- START
- RESET
- IOLOAD
- CONFIG
- RUN

While the computer is operating, host accesses to the RAM and I/O subsystems are disabled until the IDSM transitions to the RUN state of operation. Table 2-1 describes the IDSM operating states and the functions enabled for the adapter in each state. See Chapter 3 for more information about the adapter's subsystems.

Table 2-1. IDSM Operating States and Adapter Functions

IDSM State	Adapter Description	Functions
START	Initial condition.	Reads the on-board EEPROM. I/O base address and all other parameters are initialized into the PROM control register (PCR), RAM configuration register (RCR), and interrupt channel register (ICR). Disabled state. The adapter responds only to write accesses to the ID port at 100h.
RESET	Intermediate state. Entered from the START or from the RUN state through the ID pattern (see "ID Pattern Generator" in the next section).	Disabled, as in the START state.
IOLOAD	Disabled state. Allows you to program the IOBASE parameter. Entered from the RESET state.	Disabled. Allows software to override the I/O base address read from the EEPROM. The next write to the ID port is interpreted as an I/O base address override. If the value is 0FFh, no override occurs.
CONFIG	Enables adapter's I/O accesses. Entered from the IOLOAD state.	I/O accesses enabled. Configuration registers PCR, RCR, and ICR are enabled for read or write operations. See "RAM Configuration Register (at Offset E)" in Chapter 3. Software can override configuration parameters in these registers. Software can also write configuration parameters into the on-board EEPROM (non-volatile memory).
RUN	Enables all of the adapter functions except reconfiguration. Entered from the CONFIG state.	Enabled. All adapter functions are enabled. The adapter is configured according to the current value in the configuration registers. The configuration registers are read-only. See Chapter 3 information about the adapter's subsystems and registers.

Each time the adapter is reset or the RST bit (bit 7 at offset 6) in the EEPROM control register is set, the IDSM resets to its initial condition (START). In the START state, the adapter is in a non-operating or disabled state, as described in Table 2-1. The RST bit resides in the adapter's control register.

ID Pattern Generator

The ID pattern generator in the adapter's driver and configuration program produces an exact sequence of 255 byte values to which the IDSM responds. Each time the ID pattern generator advances the IDSM to the next state, the IDSM transitions the adapter to its next state of operation. The IDSM changes the operating state of the adapter after a sequence of specific I/O write operations are issued from the host computer. Figure 2-2 shows the algorithm used by the ID pattern generator.

```
MOV DX, 100h
    MOV   CX, 0FFh
    MOV   AL, 0FFh
@@1:
    OUT   DX, AL
    SHL   AL, 1
    JNC   @@2
    XOR   AL, 0E7h
@@2:

    LOOP  @@1
```

Figure 2-2. ID Pattern Generator Algorithm

Whenever a 00h is written to the ID port, the corresponding hardware pattern generator in the gate array is reset to its initial condition of FFh (START). The adapter's configuration registers are loaded from the EEPROM and the adapter is disabled for other functions.

NOTE: The ID port location (100h in the I/O base register) is fixed and cannot be changed. It may conflict with other installed devices such as the Banyan® VINES® Advanced Intelligent Communications Adapter (ICA™). Refer to the documentation that accompanied the conflicting adapter for more information.

The ID pattern generator advances the IDSM to the next state (RESET) in the sequence (see the algorithm in Figure 2-2) which resets control register at offset 6. The adapter remains in the disabled condition, and the algorithm advances the IDSM to the IOLOAD state.

If a non-matching value is written to the ID port before the sequence finishes, the ID pattern generator resets the IDSM to its initial condition (the START state). The hardware signal LAST is asserted when the hardware pattern generator is in its last state (the RUN state at 8Ch).

IDSM Programming Notes

A device driver usually enables the adapter by sequencing the ID state machine to the RUN state by writing the sequence shown in Figure 2-3 to the ID port at 100h, bit 0 in the I/O base address register (Figure 2-5 shows the I/O base address register in the IOLOAD state).

```
0
ID pattern
0
```

Figure 2-3. Sequence for Enabling the RUN State

The configuration utility enables the adapter by sequencing the IDSM through the IOLOAD state to the CONFIG state at offsets D, E, and F from the I/O base. This transition resets the control register at offset 6 and enables the adapter for I/O accesses only by writing the sequence shown in Figure 2-4 to the ID port.

```
0
ID pattern
ID pattern (the adapter is now in IOLOAD state)
Adapter I/0 base address
```

Figure 2-4. Sequence for Enabling the CONFIG State

When the ID state machine is in the IOLOAD state, the next I/O write to the ID port loads the I/O base address register, the ID port, write only, if the data is not equal to FFh (current ID sequence value). Figure 2-5 shows the I/O base address register in IOLOAD state.

7	6	5	4	3	2	1	0
*	*	*	IO4	IO3	IO2	IO1	IO0

IO4-0 : IO base address = (value) 10h + 0200h

Figure 2-5. I/O Base Address Register in IOLOAD State

After the I/O base address write, the adapter is in the CONFIG state. I/O accesses are enabled and the PCR, RCR, and ICR configuration registers are enabled for write operations.

NOTE: Memory accesses and interrupts remain disabled in the CONFIG state.

If the state of the adapter is unknown to the software, the software writes the sequence shown in Figure 2-3 to the ID port to ensure the adapter is in the RUN (fully operational) state. All the adapter's functions are enabled in the RUN state: I/O accesses, memory accesses, and interrupts.

Chapter 3
Adapter Subsystems

This chapter provides a functional description of the adapter's subsystems.

ROM Subsystem

The adapter is factory configured with no boot ROM present. When installing a ROM on the adapter, set the ROM base address and window size using the configuration utility on the *EtherDisk* diskette. The ROM base address is mapped into host address space and takes effect after a reset. The software configured ROM size must match the hardware ROM size.

CAUTION: Do not map the ROM window base over the video bios, typically 0C 0000h to 0C 6000h depending on your computer. Refer to the user's manual that accompanied the computer for specific information.

The ROM base addresses in the 16- to 24-KB range are unusable if the adapter's ROM size is set to 32 KB.

RAM Subsystem

The RAM is dual-ported between the 82586 controller and the Industry Standard Architecture (ISA) bus (refer to Figure 2-1 in Chapter 2). It uses two 70 ns, 32 KB x 8 SRAM chips (64 KB). The RAM decode logic decodes the unlatched address (LA) and system address (SA) lines. It drives the –MEMCS16 bus signal into the RAM arbitration logic.

The RAM control logic arbitrates memory access between the ISA bus and the 82586 bus cycles using the RAM decode signal, unqualified by any memory/IO information. The 82586 controller may occasionally defer to an ISA memory access.

Address Mapping

The 64-KB RAM appears in the host memory address space between 0C 0000h and 0D FFFFh, or F0 0000h and F9 FFFFh on protected mode systems depending on how the adapter is configured. The RAM appears in the 82586's configurable address space at 0000h through FFFFh. If the RAM is mapped to one of the protected mode addresses (F0 0000h through F8 0000h), the RAM window size remains 64 KB, but 128 KB of host address space is used. Select from 16 KB to 64 KB for window size. If you choose any size smaller than 64 KB, the remaining RAM space on the adapter is unavailable to the host. The RAM address is adjusted so that the last byte of the RAM accessible by the host appears at address FFFFh in the 82586's address space.

NOTE: When using either the EtherStart®16 boot PROM (3Com part #3C507-ES) or the NetWare® Boot PROM (3Com part #3C507-NW) with the IBM PS/2 Model 30, the RAM base must begin at a lower address than the ROM base.

Since the RAM and ROM base address options have many of the same available settings, be sure that they are set to different values on the adapter and that they do not conflict with each other or any other devices.

System Address Decode (SAD) Mode

The EtherLink 16 and EtherLink 16 TP adapters provide a 64-KB or smaller buffer window. According to the ISA bus specification, when a 16-bit add-in memory device is installed in a 128-KB range, 8-bit devices must not reside in the same 128-KB range as the 16-bit add-in device. If other 16-bit devices cannot be configured to fill the 128-KB range, some system address space is unusable. To overcome this restriction, the adapter can be configured to respond only to memory accesses specifically intended for the on-board memory with delayed assertion of the bus control –MEMCS16 signal (through modified timing). However, data corruption can result when the adapter operates with the modified timing on the following systems:

- IBM PS/2 Model 30/286, 25/286
- Siemens® computer system
- Intel 25 MHz Intel386 MicroComputer Model 302
- VLSI Technology, Incorporated (VTI™) chipset
- WYSE® WY-2012i

The adapter provides the data mode option "STANDARD" and "TURBO" settings for correct adapter operation. The data mode option controls the SAD bit and the LAD bit in the adapter's configuration registers. See Table 3-1.

STANDARD mode is the factory setting that is selected by the EEPROM configuration. In this mode, the adapter uses 8-bit data transfers only and operates correctly. However, performance is restricted to the speed of an 8-bit device by the exclusive 8-bit transfers. With the adapter installed as a 16-bit device, you can set both the SAD and LAD bits to 1 to enable the STANDARD setting implemented by the driver software. In this case, the adapter responds only to a 128-KB range of addresses. The software ensures that no accesses are generated within the range that are outside of the true buffer size.

TURBO mode can be used on machines that allow the modified ISA bus sequencing. In TURBO mode, the adapter operates as a full 16-bit device. Most personal computers support this mode.

NOTE: Test the adapter with the TURBO setting to ensure that it operates in the computer. If the adapter does not operate correctly with the TURBO setting, use the configuration utility to reset the data mode option to the STANDARD setting.

16-bit data transfers can operate when the factory-set STANDARD mode (referred to as the STANDARD/16 mode) is selected. However, the driver software must ensure that interrupts are disabled and that the LAD bit is set to ON before the transfers begin. The software must reset the LAD bit to 0 and enable interrupts.

Table 3-1. SAD and LAD Bit Locations

	Register/Offset	Bit
SAD	RAM Configuration/E	6
LAD	Control/6	4

NOTE: The SAD bit can be set only while the IDSM is in the CONFIG state.

Use the algorithm shown in Figure 3-1 to enable the STANDARD mode with 16-bit data transfer capibility (STANDARD/16 mode).

```
Disable CPU interrupts.
Set the LAD bit (=1) to enable 16-bit transfers.
Do a rep mov.
Clear the LAD bit (=0) to disable 16-bit transfers.
Enable CPU interrupts.
```

Figure 3-1. STANDARD/16 Mode Algorithm

NOTE: When the SAD and LAD bits are both on (=1) and the adapter is in the 128-KB range, the adapter responds to any memory access in the 0C 0000h to 0D FFFFh address range. Interrupts must be disabled to prevent other memory accesses in this range.

The software can read the value of the SAD bit from the RAM configuration register to determine if the STANDARD/16 mode algorithm is required for 16-bit accesses. Table 3-2 describes the SAD and LAD bit settings.

Table 3-2. Data Access and SAD/LAD Bit Settings

Data Access	Mode Name	SAD Bit	LAD Bit	Notes
8-bit	STANDARD	1	0	Factory setting. Reliable access mode, but the adapter performance is slower than that provided by a 16-bit mode.
16-bit	STANDARD/16	1	1	16-bit data transfers are enabled by the driver software. The adapter responds to a 128-KB range of addresses. Software must ensure that no accesses are generated within the 128-KB range.
16-bit	TURBO	0	X	Allows 16-bit setting accesses to the adapter buffer, but can cause data corruption if used on some types of computers (listed earlier in this chapter).

I/O Subsystem

The I/O subsystem handles ISA bus accesses to the boot ROM, network management data ROM, and all the control, status, and configuration I/O registers. All accesses to this subsystem are 8-bit. This logic does not assert –MEMCS16, IOCS16, or 0WS.

Figure 3-2 shows the I/O register set where the register number is offset from the I/O base.

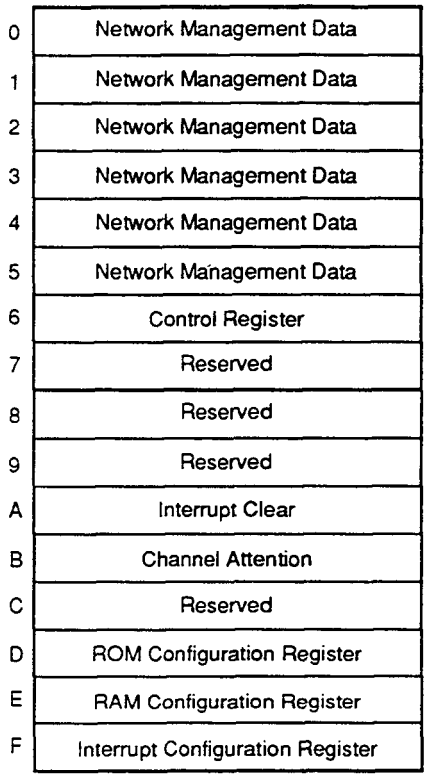

Figure 3-2. I/O Register Set

Network Management Data (Offset 0-5, Read-only)

Two bits in the control register at offset six select the six-byte bank of data that appears in offset 0 through 5 (network management data) as read-only data. The four banks are listed in Table 3-3.

Table 3-3. Network Management Banks at Offset 0 through 5

Bank	Data Type	Control Register Bit 1	Bit 0
1	3Com adapter signature *3COM* in ASCII	0	0
2	Ethernet address is in hex (in packed BDC)	0	1
3	3Com part number	1	0
4	Reserved	1	1

Control Register (Offset Six)

Figure 3-3 shows the control register at offset six, where the default is equal to zero, and read and write are enabled.

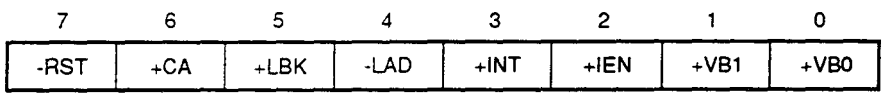

Figure 3-3. Control Register at Offset Six

Table 3-4 describes the bits in the control register at offset six.

Table 3-4. Bits in the Control Register at Offset 6

Bit	Setting	Description
–VB1		Network Management Data bank select (R/W).
+VB0	00	3Com signature = "*3COM*."
	01	Ethernet Address.
	10	Adapter part number and revision level.
	11	Reserved.
+IEN		Interrupt enable (R/W). Enable the assertion of a host system interrupt by the 82586.
+INT		Interrupt latch active (R). The 82586 is signaling an interrupt condition. This latch can only be cleared by an I/O write to offset A.

(continued)

Table 3-4. Bits in the Control Register at Offset Six (continued)

Bit	Setting	Description
LAD	0	LA address decode disable; no effect if SAD bit is disabled (R/W). If SAD bit is enabled and RC5 is disabled, the adapter responds as an 8-bit device (does not drive –MEMCS16). Enables LAD bit and allows the adapter to respond as a 16-bit device (drives –MEMCS16).
+LBK	0	Normal network operation. Loopback enable (R/W). Setting the loopback bit causes the assertion of the LBK signal to the encoder/decoder.
+CA		Channel Attention (R/W). Setting the channel attention bit causes the assertion of the CA signal to the 82586. The register must be set and cleared via the software to provide the channel attention signal to the 82586. Using the channel attention register (offset B) is faster. The +CA resister is retained in the adapter for compatibility with the EtherLink/MC.
–RST:	0	82586 reset (R/W). Setting the 82586 reset bit to ZERO (0) causes the assertion of the 82586 reset signal (RESET).

Figure 3-4 shows a sample assembly code fragment that illustrates how to initialize the adapter and read the Ethernet address. Refer to Figure 2-2 for the ID pattern algorithm required to program the adapter. Refer to Table 3-3 for an explanation of the network management banks at offset 0 through 5.

```
:   go to RESET state       ;transition IDSM to RESET state
    go to IOLOAD state      ;write the ID pattern algorithm
    go to CONFIG state      ;write the ID pattern algorithm
                            ;to initialize the adapter
then:
    MOV   DX ,  IOBASE
    ADD   DX ,  6           ;add the control register
    IN    AL ,  DX          ;read from the control register
    AND   AL,   0FCH        ;
    OR    AL,   01H         ;
    OUT   DX,   AL          ;select the Ethernet address bank
                            ;(Net Management bank 2, bits 1 and 0)
    MOV   CX,   6
    SUB   DX,   6
lp: IN    AL,   DX

    MOV   [store| AL
           queue]
    INC         DX

    loop        lp
```

Figure 3-4. Sample Assembly Code Fragment for Network Management Banks at Offset 0 through 5

Interrupt Clear Register (Offset A, Write-only)

Any write to this register clears the interrupt latch.

Channel Attention Register (Offset B, Write-only)

Any write to this register causes the channel attention (CA) signal to be asserted to the 82586 for two 82586 clock times and then deasserted. The CA bit (bit five in the control register) is also used for this purpose, but must be set and then cleared to assert, then deassert the CA signal.

ROM Configuration Register (Offset D)

Figure 3-5 shows the ROM configuration register at offset D, read-only in RUN state, read/write in CONFIG state.

CAUTION: If the ROM window size is set to any valid value other than zero, then the mapping is enabled in all states of the adapter. If the ROM window size is set to a value other than zero, ensure that the ROM window base address does not cause configuration conflicts. Do not map the ROM window base over the video bios, typically C0000h to C6000h, depending on the computer. Refer to the user's manual that accompanied the computer for specific information.

7	6	5	4	3	2	1	0
XCVR	P8*	PC5	PC4	PC3	PC2	PC1	PC0

* P8 is reserved for factory testing. Always write it to zero.

Figure 3-5. ROM Configuration Register at Offset D

Table 3-5 lists the ROM window sizes.

Table 3-5. ROM Window Sizes, PC1 through PC0 at Offset D

Setting	ROM Window Size
00	No boot ROM present in system
01	08 KB
10	16 KB
11	32 KB

Table 3-6 lists the settings for the ROM window base addresses PC5 through PC2 at offset D.

Table 3-6. ROM Window Base Addresses, PC5 through PC2 at Offset D

Setting	ROM Window Base Address (h)	Setting	ROM Window Base Address (h)
0000	0C 0000	1000	0D 0000
0001	0C 2000	1001	0D 2000
0010	0C 4000	1010	0D 4000
0011	0C 6000	1011	0D 6000
0100	0C 8000	1100	0D 8000
0101	0C A000	1101	0D A000
0110	0C C000	1110	0D C000
0111	0C E000	1111	0D E000

Table 3-7 lists the settings for the ROM configuration register at bit seven, which selects the transceiver type for the adapter:

Table 3-7. Transceiver Settings, ROM Configuration Register at Bit Seven

	Transceiver Type	ROM Config. Setting	State
EtherLink 16	On-board BNC	0	Disabled
		1	Enabled
	External AUI	1	Disabled
		0	Enabled
EtherLink 16 TP	On-board twisted-pair	1 or 0	Enabled

RAM Configuration Register (Offset E)

Figure 3-6 shows the RAM configuration register at offset E. RUN state at offset E is read-only. The CONFIG state is read/write.

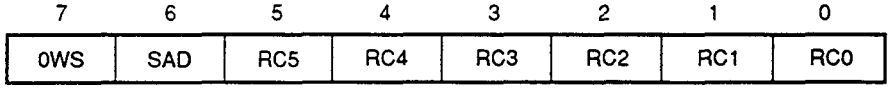

Figure 3-6. RAM Configuration Register at Offset E

Table 3-8 lists the RAM configuration window base and window size settings at offset E, registers RC5 through RC0.

CAUTION: Use only the settings listed in Tables 3-8 and 3-9 for the adapter to operate properly.

High addresses (F0 0000h through F8 0000h) require protected-mode processors and drivers. Although the window size is 64 KB, the adapter maps over 128 KB of address space and responds for either value assigned to address bit 16.

Table 3-8. RAM Configuration Registers RC5 through RC0 at Offset E

RC5-RC0 Value (h)	Window Base (h)	Window Size (h)
00 0000	0C 0000	16 KB
00 0001	0C 0000	32 KB
00 0010	0C 0000	48 KB
00 0011	0C 0000	64 KB
00 1000	0C 8000	16 KB
00 1001	0C 8000	32 KB
00 1010	0C 8000	48 KB
00 1011	0C 8000	64 KB
01 0000	0D 0000	16 KB
01 0001	0D 0000	32 KB
01 0010	0D 0000	48 KB
01 0011	0D 0000	64 KB
01 1000	0D 8000	16 KB
01 1001	0D 8000	32 KB
11 0000	F0 0000	64 KB
11 0001	F2 0000	64 KB
11 0010	F4 0000	64 KB
11 0011	F6 0000	64 KB
11 1000	F8 0000	64 KB

Table 3-9 lists the configuration settings required for bits seven and six at offset E, Zero Wait State (0WS) and SAD, respectively.

Table 3-9. Zero Wait State (0WS) and SAD RAM Configuration Register, Bits Seven and Six at Offset E

Bit	Setting	Bit-Slot Size	Description	Notes
7	0	16	0WS disabled.	—
	1		0WS enabled.	Data transfer uses two bus clock cycles instead of three.
	0	8	2WS enabled.	Data transfer uses four bus clock cycles instead of six when 2WS is enabled. 0WS is not asserted with the adapter installed in an 8-bit slot in the computer.
6	0	n/a	SA address decode enabled.	SA address decode (SAD-bit) enabled for normal adapter operation.
	1	n/a	SA address decode enabled.	SA address decode disabled. No effect if the RC5 bit in the RAM configuration register offset E is ON. See Figure 3-6 .

Notes on RAM Configuration at Offset E

The configuration program ensures that only valid values are used.

- RAM addressing is adjusted by the adapter so that the last byte of the RAM window accessible by the host always appears at address FFFFh in the 82586's address space regardless of the RAM window size.
- Observe the settings in Tables 3-8 and 3-9 for proper operation of the adapter.
- When using high-memory addresses above 15 MEG, the adapter must ensure no other memory accesses are permitted starting at the adapter's ROM base address.
- Values not listed in Table 3-9 (bits 0 through 5) are reserved.
- SAD must be asserted in the IBM PC Model 30 286 and computers based on the VLSI Logic 8000-series VTI chipset. Refer to the manual that accompanied your computer or contact your network supplier for information.
- 0WS should be disabled in an IBM PC AT.

Interrupt Configuration Register (Offset F)

Figure 3-7 shows the interrupt configuration register that appears at offset F. The RUN state at offset F is read-only. The CONFIG state is read/write.

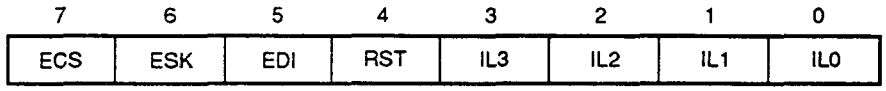

Figure 3-7. Interrupt Configuration Register at Offset F

Table 3-10 desribes the bits in the interrupt configuration register that appears at offset F and their corresponding values.

Table 3-10. Interrupt Configuration Register at Offset F, Bit Values

Bit	Value/Description
IL3-0:	Interrupt request level select. See Table 3-11 for a list values.
RST/EDO:	RST restarts the board configuration logic. EEPROM is reread and the control register is reset to zero (0). RST is Write, EDO is Read. Set to 0: No action. Set to 1: Restart board configuration.
EDO:	Serial data from the EEPROM.
EDI:	Serial data into the EEPROM.
ESK:	Shift clock to the EEPROM.
ECS:	Chip select to the EEPROM.

Table 3-11 lists the valid interrupt request levels (bits 3 through 0 in the interrupt configuration register at offset F) and their values. Any other value deselects all interrupts.

Table 3-11. Interrupt Configuration Register, Bits 0 through 3 at Offset F

IR Level	Value
3	0011
5	0101
7	0111
9	1001
10	1010
11 *	1011
12	1100
15	1111

* Supported on EtherLink 16 adapter, revision level - 05 and later and on all revisions of the EtherLink 16 TP adapter.

Test Mode

Each time the TEST point is pulled to +5V on the EtherLink 16 adapter , or to 0V on the EtherLink 16 TP adapter, a fixed configuration is shifted into the configuration registers instead of out of the EEPROM. The adapter automatically transitions into the CONFIG state and receives the factory settings for each software configuration option. The TEST mode signal is sampled whenever the adapter's configuration logic is reset. Table 3-12. lists the TEST mode configuration for the adapters.

Table 3-12. Test Mode Configuration

Test Mode Configuration Parameter	Test Mode Parameter Value
I/O base address	300h
OWS	0 (DISABLED)
SAD	0 (DISABLED)
XCVR	1 (ON-BOARD enabled*)
Interrupt level	3
Boot ROM base address	0C 8000h
Boot ROM size	00
Packet RAM base address	0D 0000h
Packet RAM size	64-KB
Data Mode	0 (STANDARD)

* BNC transceiver on EtherLink 16 only. For EtherLink 16 TP, the TEST mode configuration (the factory setting) is internal to the adapter (RJ45), and cannot be changed.

EEPROM Subsystem

The EEPROM logic shifts configuration data out of the EEPROM and into the adapter configuration registers each time the board configuration logic is reset (the adapter is reset or the RST bit in the ICR is written). Exactly 32 bits (two EEPROM words) are transferred. Figure 3-8 shows the format in which the data must be stored in the EEPROM.

NOTE: Data must be written into the EEPROM using bits five, six, and seven of the interrupt configuration register (offset F).

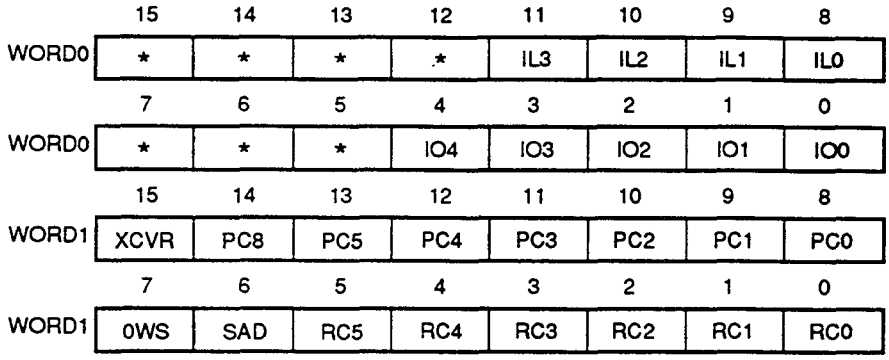

Figure 3-8. EEPROM Configuration Data Storage Format

To program the EEPROM, see the National Semiconductor 9306 data sheet for detailed information.

Transceivers

Table 3-13 lists information about the transceivers for each of the adapters.

Table 3-13. EtherLink 16 and EtherLink 16 TP Adapter Transceivers

	EtherLink 16	EtherLink 16 TP
On-Board Transceiver	10BASE2 Ethernet transceiver with BNC connector.	10BASE-T twisted-pair with RJ45 connector.
External Transceiver	AUI Ethernet connector.	Not applicable.
Implementation Method	National Semiconductor 8391 encoder/decoder chip.	MicroLinear ML4658 10BASE-T semi-custom transceiver chip.
IEEE Specification/ Collision Levels	802.3 specification.	802.3i 10BASE-T standard.
Factory Setting	On board user alterable.	On board not user alterable.
Selection Method	Software option setting.	Software option and jumper settings can be altered for pre-10BASE-T compatibility.
Installation Reference	3Com part #6847-xx.	3Com part #7514-xx.

Chapter 4
Technical Specifications

This chapter lists the technical specifications for the adapter including RFI and safety issues, physical dimensions, power requirements, and environmental conditions.

RFI and Safety Issues

The EtherLink 16 adapter meets the following limits:

- Certified, FCC Rules, Part 15, class B digital device
  FCC ID #: DF67CC3C507
- VDE 0871 Vfg 1046/1984, class B
- UL 478, fifth edition

The EtherLink 16 TP adapter meets the following limits:

- Compliance with FCC Rules, Part 15, class B digital device
- UL 1950, fifth edition

Physical Dimensions

The EtherLink 16 adapter has the following external dimensions:

Length	9.0 inches (22.9 cm)
Width	4.2 inches (10.7 cm)

The EtherLink 16 TP adapter has the following external dimensions:

Length	9.4 inches (23.9 cm)
Width	4.2 inches (10.7 cm)

Power Requirements

	Amps Max.	Volt Tolerances
EtherLink 16	2.0	+5 ± 5%
	0.2 Internal Transceiver (XCVR=1)	+12 ± 10%
	0.5 External Transceiver (XCVR=0)	+12 ± 10%
EtherLink 16 TP	0.05	-5 ± 5%
	0.2 Internal Transceiver (XCVR=1)	+5 ± 10%

Environmental Conditions

During operation, the adapter requires the following environmental conditions:

Humidity	10% to 90% noncondensing	
Altitude	0 to 10,000 ft. (approx. 3,000 m)	
Temperature	**EtherLink 16** 0 to 70° C	**EtherLink 16 TP** 0 to 55° C

Appendix A
Programming Guidelines for the Adapter Driver

The EtherLink 16, EtherLink 16 TP, and EtherLink/MC (3C523) adapters each use a memory-mapped architecture, Intel's 82586 network controller chip, and a software register-based adapter function control. You can modify existing EtherLink/MC code to set up and maintain the 82586 control structures for the EtherLink 16 or EtherLink 16 TP adapter. Use the procedures in this appendix to modify the EtherLink/MC adapter driver software.

Modifying EtherLink/MC Driver Software

Follow this procedure to modify the EtherLink/MC driver software for the EtherLink 16 and EtherLink 16 TP adapter:

1. **Revise the initialization logic so that it obtains configuration information from the RUN state registers.**

   The EtherLink/MC adapter obtains configuration information from POS registers, and the EtherLink 16 and EtherLink 16 TP adapters obtain the information from the RUN state registers. Modify the EtherLink/MC initialization logic so that the adapter obtains the appropriate information from the RUN state registers. For information about the RUN state registers, see Chapters 2 and 3, earlier in this guide.

2. **Revise use of the control register.**

   On the EtherLink/MC adapter, the meaning of the least significant two bits of the control registers points the adapter to RAM bank select. Modify the code to point to the Network Management register bank. For information about the Network Management register bank, see "Network Management Data" in Chapter 3 of this guide.

3. **Add logic to the receive interrupt handler to reset the interrupt latch.**

   The EtherLink/MC, EtherLink 16, and EtherLink 16 TP adapters handle interrupt latching differently: On the EtherLink/MC adapter, you can enable and disable the latching of interrupt lines; the line is unlatched in the factory configuration. On the EtherLink 16 and EtherLink 16 TP adapters, the interrupt line is always latched. See Chapter 3 earlier in this guide for information.

4. **Insert SAD/LAD mode logic for VTI chipset-based personal computers (for example, the IBM Model 30 286).**

   SAD/LAD mode logic does not occur in the EtherLink/MC adapter software. When you modify the EtherLink/MC code for the adapter, add the SAD/LAD mode logic. For information on SAD/LAD mode logic, see (Offset D)," and "System Address Decode Mode" in Chapter 3 of this guide.

Improving the Adapter's Performance

Once the EtherLink/MC adapter software is modified for the adapter, complete the following optional steps to improve the adapter's performance:

1. **Replace the EtherLink/MC control register-based Channel Attention logic with the Channel Attention register.**

   On the EtherLink/MC, channel attention logic resides in the control register. On the EtherLink 16 and EtherLink 16 TP adapters, there is a separate Channel Attention register. See "Control Register (Offset 6)" for a description of the +CA bit, and "Channel Attention Register (Offset B, Write-only)" in Chapter 3 of this guide.

2. **Modify the EtherLink/MC RAM map logic to use the same amount of RAM as is configured for the EtherLink 16 or EtherLink 16 TP adapter RAM.**

   The EtherLink/MC provides 16 KB of RAM, which is used by the EtherLink 16 or EtherLink 16 TP adapter in the first five modifications listed in this appendix (steps 1 through 4 in "Modifying EtherLink/MC Software," and step 1, above). The EtherLink 16 and EtherLink 16 TP adapters use only the first 16 KB of the 64 KB of packet buffer RAM when you complete these modifications. Modify the RAM map logic so that your adapter can access and use as much RAM space as possible.

   See "RAM Configuration Register (Offset E)" in Chapter 3 of this guide for information about the RAM configuration register.