ERRATA SHEET for Revision A of the MUAA2K80 RCP

Device
MUAA2K80 Routing CoProcessor
Product Revision: A

Problem
The SYNC port does not assert /DINREADY when a cycle from the Processor port or an auto-age event occurs and there is an operation already waiting in the SYNC port pipeline. This causes the pending cycle in the SYNC port pipeline to be overwritten by the next SYNC port cycle. This bug affects the operation of the MUAA whether the SYNC port has higher priority or not.

Scope
This problem affects all applications that use either of the following device features:
- Auto-age;
- Simultaneous use of the SYNC port and Processor port.

Fix
A fix is being developed, and MUAA2K80 Rev. B silicon should be available June 30, 1999. This bug will not affect the MUAA8K80.

Workaround
The following techniques may be used to work around the problem:

1. Do not use the auto-age feature. Aging instructions may be run from the Processor port or the SYNC port at the required interval. The Entry Life register is programmed the same as before.

2. It is necessary to prevent access to the CAM core on the SYNC port and the Processor port simultaneously. The MUAA will function properly when using both ports if these guidelines are followed:

   A) The rising edge of /PCS (that is the end of the PCS cycle) may occur any time after the rising edge of CLK that starts the last SYNC port operation. /DINE should be HIGH to disable the SYNC port, until the guidelines in B are met. Note that this implies that the /PCS cycle may start while the SYNC port is in use, as long as the cycle completes after the last SYNC port accepts the last operation.

   B) The next SYNC port operation should not be started until the seventh rising edge of CLK following the rising edge of /PCS. LOAD cycles do not start an operation, therefore they may be used during this interval.

The SYNC port may be run fully pipelined provided the /DINREADY signal regulates the flow of DIN data and the Processor port does not get core access while the SYNC port is operating. Not all Processor port operations affect the core. Only accesses to Registers 0 and 2 through 12 need external arbitration as outlined above. Access to Registers 1 (LOAD) and 13 (DOUT) through 28 may occur without regard to the status of the SYNC port.

These workarounds will not be required with MUAA2K80 Rev. B silicon or the MUAA8K80.

Additional Information
Release 0.9 Beta of the MUAA device models correctly reflects the operation of the Rev. A silicon, including the problems with the arbiter. The model will be updated when the fix is available.

Please contact MUSIC Applications Engineering if you have further questions.

NOTES

MUSIC Semiconductors Agent or Distributor:

MUSIC SEMICONDUCTORS

http://www.music-ic.com
email: info@music-ic.com

Worldwide Sales Headquarters
MUSIC Semiconductors
4633 Old Ironsides Drive • Suite #130
Santa Clara, California 95054 USA
Tel: 408-330-7550
Fax: 408-330-7559
USA Only: 800-933-1550 Tech. Support
888-226-6874 Product Info.

Asian Sales Office
MUSIC Semiconductors
Special Export Processing Zone 1
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 49 549 1480
Fax: +63 49 549 1024
Sales Tel/Fax: +632 723 62 15

European Sales Office
MUSIC Semiconductors
P.O. Box 184
6470 ED Eygelshoven
The Netherlands
Tel: +31 45 546 2177
Fax: +31 45 546 3663