MU9C8338/8358L Ethernet Filter Interface Errata Sheet

AFFECTED DEVICES

MU9C8338 Revision C and MU9C8358L Revision A Ethernet Filter Interfaces.

PROBLEM 1

/FI input expects a 0 to 1 transition in order to cause the Full Flag interrupt, while the LANCAM /FF output goes from 1 to 0 when a CAM Full condition occurs.

Scope

This problem affects applications where the Full Flag Interrupt is enabled in the System Target register (STARG) with bits [1:0] = 10.

Fix

No silicon changes are currently planned to correct this problem but future changes are possible.

Workaround

MUSIC recommends that all designs requiring the Full Flag interrupt have an inverter placed between the /FF output and /FI input. If the inverter is obtained from logic other than a programmable logic device, a 0-Ohm bypass resistor is recommended so the PCB will be compatible with any later revisions. In the example shown in Figure 1, R1 is installed and R2 is omitted. If the inverter is not required and can not be removed from the PCB, resistor R1 can be omitted and R2 installed.

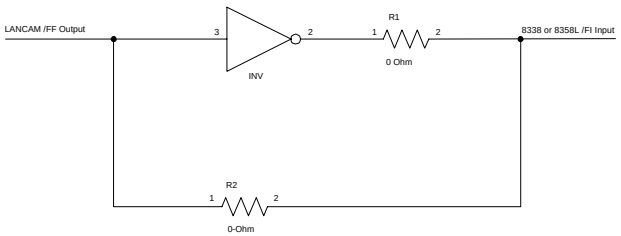

Figure 1: LANCAM /FF Signal Inverter Workaround

Documentation

The installation of the inverter, described in the workaround section of this errata, requires a minor clarification to the Data Sheet. Table 2 on page 10 of the 8353L Data Sheet and Table 2 on page 5 of the 8338 Data Sheet should be changed as shown in bold in Table 1 and Table 2 while using the workaround.

Table 1: Previous

STARG	SSTAT. Please note that /INTR will only return HIGH when the LANCAM has become not full. Therefore, after the SSTAT register read has confirmed the status of the interrupt condition, an entry should be removed from the LANCAM by using the PURGE sequence.	The /FF output from the LANCAM(s) has indicated that the LANCAM is full. When reading the SSTAT register, a full condition is indicated by **bit 0 = 0.**

Table 2: Revision After Workaround

STARG	SSTAT. Please note that /INTR will only return HIGH when the LANCAM has become not full. Therefore, after the SSTAT register read has confirmed the status of the interrupt condition, an entry should be removed from the LANCAM by using the PURGE sequence.	The /FF output from the LANCAM(s) has indicated that the LANCAM is full. When reading the SSTAT register, a full condition is indicated by bit **0 = 1 due to the inverter.**

PROBLEM 2

After setting the System Target register (STARG) appropriately, the method for resetting the Full Flag interrupt does not function as it is described in the data sheet. Once a Full Flag interrupt has occurred, it should reset once the System Status register (SSTAT) is read and the LANCAM has been made not full by removing an entry. A problem exists that causes the /INTR pin to remain at logic 0 although the interrupt condition has been removed and the appropriate registers have been read.

Scope

This problem affects applications where the Full Flag Interrupt is enabled in the STARG register with bits [1:0] = 10.

Fix

No silicon changes are currently planned to correct this problem but future changes are possible.

Workaround

The Full Flag Interrupt condition can be reset once it has occurred by reading an additional register. Although the additional register is not related to the condition, it will cause the /INTR pin to return to its initial state once it is read. The new procedure to reset the interrupt condition is as follows:

1. Read System Status register (SSTAT) to determine Full Flag condition.
2. Remove at least one LANCAM entry using purge routine.
3. Repeat steps 1 and 2 until reading SSTAT reveals the LANCAM is no longer full.
4. Read the Result Data register (RDAT) which causes the /INTR pin to return to normal state. The contents of the register should be ignored as the action of reading the register is enough to reset the condition.

PROBLEM 3

After setting the Port Target register (PTARG) appropriately, the method for resetting the interrupt caused by a DA processing function is not as it is described in the data sheet. This problem exists for the single port in the MU9C8338 and for all four ports in the MU9C8358L. Once an interrupt has occurred, it should reset only when all possible Result data has been read from the Result Data register (RDAT). A problem exists that causes the /INTR pin to return to logic 1, regardless if there is Result data still available to be read.

Scope

This problem affects applications where the DA processing Interrupt is enabled in the Port Target register (PTARG) with bits [5:4] = 10. The problem affects the PTARG register in the MU9C8338 and PTARG_A, PTARG_B, PTARG_C, and PTARG_D in the MU9C8358L.

Fix

No silicon changes are currently planned to correct this problem but future changes are possible.

Workaround

The workaround for this problem is quite straightforward. The new procedure to reset the interrupt condition is as follows:

1. Read the Result Status register (RSTAT) to determine if there is a result in the RDAT register.
2. Read the RDAT register to retrieve the data. This will reset the Interrupt condition and therefore cause the /INTR pin to return to logic 1.
3. Read the RSTAT register to confirm if there are further results to be read from the RDAT register. If so, repeat steps 2 and 3 until RSTAT confirms there is no remaining Result data. If not, there is no further action required.

PROBLEM 4

After setting the Port Configure register (PCFG) to enable the 10 Base - x CRC check facility, the facility does not function properly. A problem exists that causes the internal logic to miscalculate the CRC when the function is enabled. This means that the SA processing function is not performed if the CRC check is enabled.

Scope

This problem affects applications where the 10 Base - x CRC check facility is enabled in the PCFG register with bit 1 = 1.

Fix

No silicon changes are currently planned to correct this problem but future changes are possible.

Workaround

It is recommended that the 10 Base - x CRC check facility is disabled in the PCFG register with bit 1 = 0.

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