USING THE MU9C8248 FDDI SRT INTERFACE

INTRODUCTION

The MUSIC Semiconductors' MU9C8248 Source Routing Transparent interface accelerates FDDI bridges and brouters when used with the MUSIC LANCAM "A" family, provides a complete Source Routing Transparent filtering solution for National Semiconductors, AMD and Motorola FDDI chipsets, and increases bridge (brouter) performance with lowered system costs.

The MU9C8248 permits Source routing over multiple ports for full-mesh architectures, as well as for architectures using the virtual ring concept. It provides for various validity checks on the Source routing information contained in the Routing Information Field (RIF), thereby freeing valuable processor time. To give basic support for network management, the MU9C8248 keeps track of errors in the RIF and totals them in error counters for statistical purposes. The MU9C8248 parses the FDDI frames to determine whether Source routing or Transparent bridging is being used, filters the RIF, controls the MUSIC LANCAM "A" family for Transparent address filtering, and reports the results of the address comparisons to the FDDI chipsets, "glue-free." User-definable program routines, such as comparing and learning, are stored in the MU9C8248, and do not need any or minimum direct microprocessor intervention.

This Application note outlines how to apply the MU9C8248 from a hardware point of view, and gives some example routines useful for Transparent bridging, supplementing the information provided in the MU9C8248 datasheet.

CONNECTION DIAGRAMS

The MU9C8248 Connected to the NS FDDI Chipset

In Figure 1, the MU9C8248 is connected to the NS' DP83261 MAC controller and the DP83251/55 transceiver, and monitors the transceiver output data from the network, as shown in Figure 2. The MU9C8248 generates XDAMAT, SRMAT and CIP signals to tell the MAC controller chip to copy or discard a frame, as shown in Figure 3. The outputs of the MU9C8248 are high impedance when they are not active, to permit additional external address compare circuits, if desired. Since SRMAT and XDAMAT are programmed Active-HIGH, a pull-down resistor is needed. The MU9C8248 can also be used with the MACSI and Player plus Chips.

The MU9C8248 Connected to the AMD FDDI Chipset

In Figure 4, the MU9C8248 is connected to the AMD' Am79C83 MAC controller and the Am7984A transceiver, and monitors the transceiver output data from the network, as shown in Figure 5. The MU9C8248 uses XDAMAT and SRMAT signals to notify the MAC controller to copy the frame, as shown in Figure 6. XSAMAT is used to indicate the MAC controller that a matching SA was found in the frame. SRMAT, XDAMAT, and XSAMAT are all programmed Active-LOW and therefore pull-up resistors are needed.

The MU9C8248 Connected to the Motorola FDDI Chipset

In Figure 7, the MU9C8248 is connected to the Motorola' MC68838 MAC controller and the MC68837 transceiver, and monitors the transceiver output data from the network, as shown in Figure 8. The MU9C8248 uses either XDAMAT and SRMAT signals to notify the MAC controller to copy the frame or in this example ABORT to indicate to flush the frame, as shown in Figure 9. In this example the ABORT signal is connected to the MAC controller RABORT2 input, but an alternative is to connect it to the MC68839 FSI REJECT input. ABORT is programmed Active-HIGH and therefore a pull-down resistor is needed.

Filtering and learning enable/disable logic

Besides the FDDI chipset specific connections, the MU9C8248 needs some extra connections to be notified when to filter and learn addresses from the FDDI network and when to stop filtering and learning operations. This is needed to prevent the LANCAM database from getting

polluted by filtering and learning addresses of frame fragments and frames that are originated by the FDDI port to which the MU9C8248 is connected.

In the first solution the logic required should be connected to the STRIP and STOP STRIP input of the MU9C8248 whereby the logic takes care of stopping the filtering/learning operation of the MU9C8248 by asserting STRIP HIGH for one MCLK period (at the moment the local bridge port starts transmission) and upon reception of a void frame or token the MU9C8248 starts its learning and filtering operation again. By asserting the STOP STRIP input HIGH for one MCLK period the MU9C8248 could be forced to filtering/ learning operation immediately.

In the second solution the logic doesn't use the void frame at all and the starting and stopping of the filtering/learning operations of the MU9C8248 is controlled by the logic solely. For this solution the STOP STRIP input is tied HIGH while the logic controls the STRIP input.

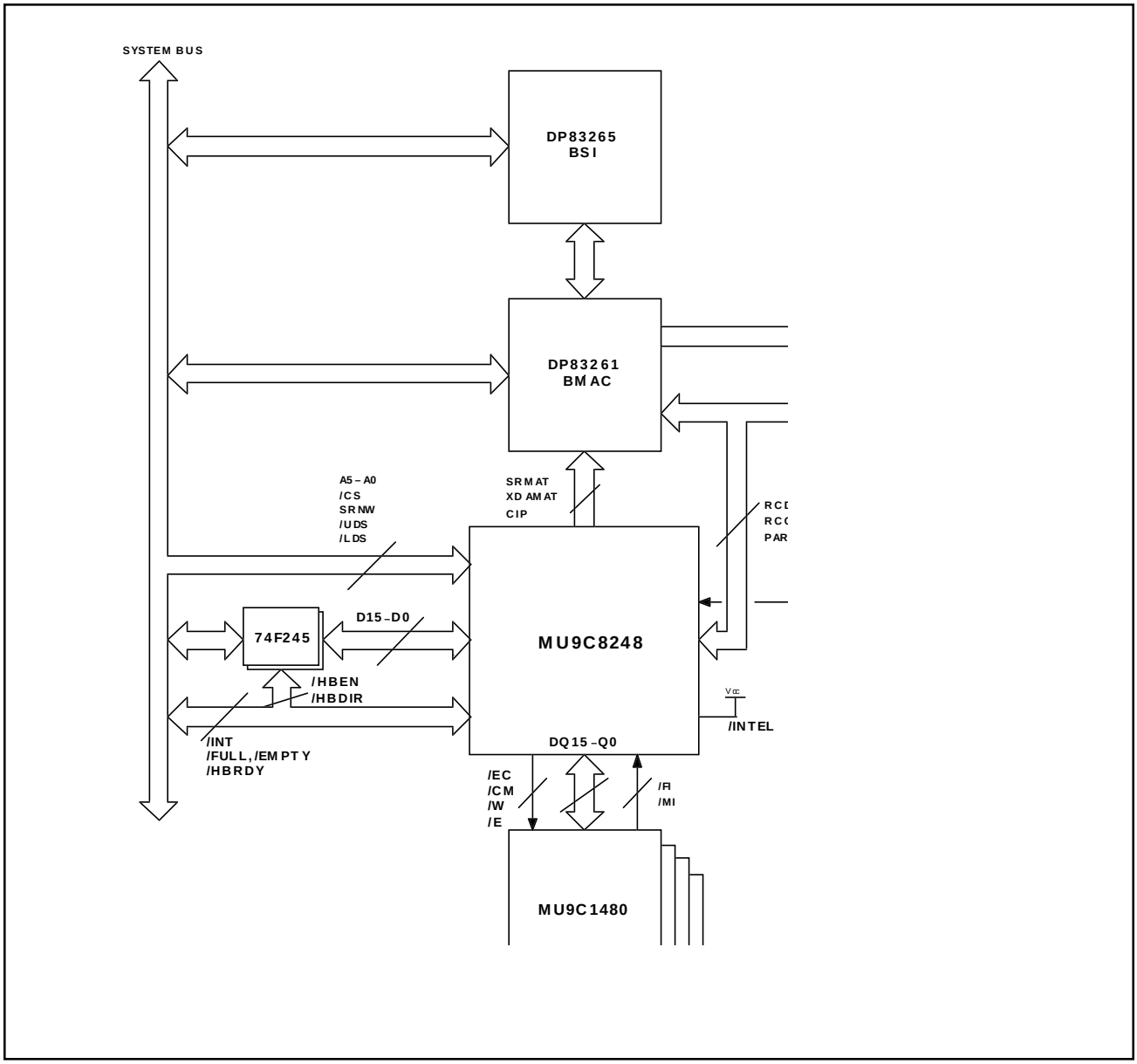


Figure 1: National Semiconductors Connection Diagram

The MU9C8248 Controlled by a Motorola Microcontroller

The MU9C8248 can be controlled by a Motorala Microcontroller when used in the Motorola addressing mode, by tying the input pin /INTEL HIGH. Signals SRNW, /LDS, and /UDS define the read and write cycles to MU9C8248 registers. A5–A0 and /CS determine which register of the MU9C8248 is accessed. The databus can be buffered by two 74F245 bi-directional buffers, which are then controlled by the /HBEN and /HBDIR signals from the MU9C8248. If the MU9C8248 needs more time for a register access, the MU9C8248 automatically stretches the microcontroller cycle by delaying /HBRDY. Outputs /INT, /FULL, and /EMPTY can be used by the microcontroller system to schedule the accesses to the MU9C8248. A detailed connection diagram to the Motorola environment is shown in Figure 10.

The MU9C8248 Controlled by an Intel Microcontroller

The connection of the MU9C8248 to an Intel environment or a Motorola environment only differs for the signals that indicate the microcontroller cycle. In the case of an Intel environment, the /INTEL pin is grounded, and the ALE, /RS and /WS signals determine the microcontroller cycle. All the other signals as described for the Motorola environment keep their functionality as mentioned. A detailed connection to the Intel environment is shown in Figure 11.

The MU9C8248 Connected to the LANCAM "A" Family

The MU9C8248 uses the LANCAM "A" FamilVy to do the address compare necessary for Transparent bridging. The MU9C8248 provides all the control needed for the LANCAM interface in either a single LANCAM or multiple LANCAM configuration, as shown in Figure 12. No additional components are needed to couple the devices.

PROGRAMMING EXAMPLES FOR THE MU9C8248

First Example

MU9C8248 Initialization

For this example, the MU9C8248 is used in an SRT bridge on a port level, using the NS chipset. For the sake of this example, the port containing this interface is connected to ring number 123H, while three other ports of this bridge are connected to ring number 456H through bridge number 6H, ring number 789H through bridge number 5H, and ring number 076H through bridge number 9H. The MU9C8248 is set up to perform negative filtering with a LANCAM database size of 2k entries.

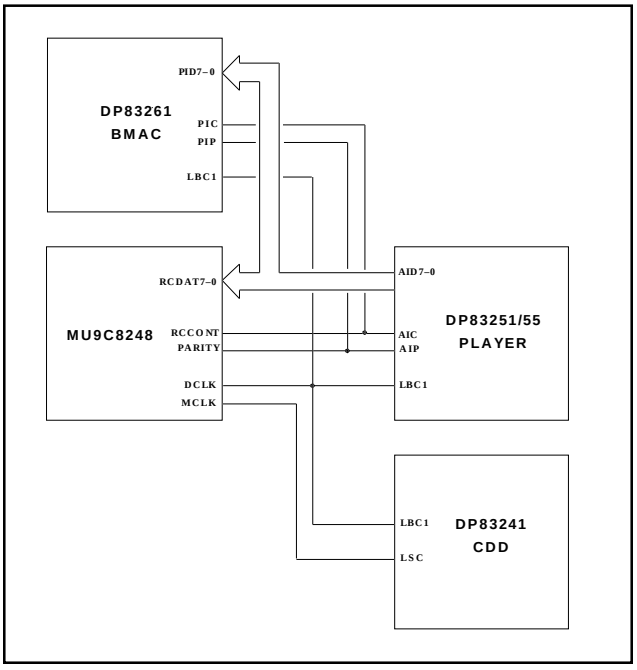


Figure 2: NS Transceiver Connection Diagram

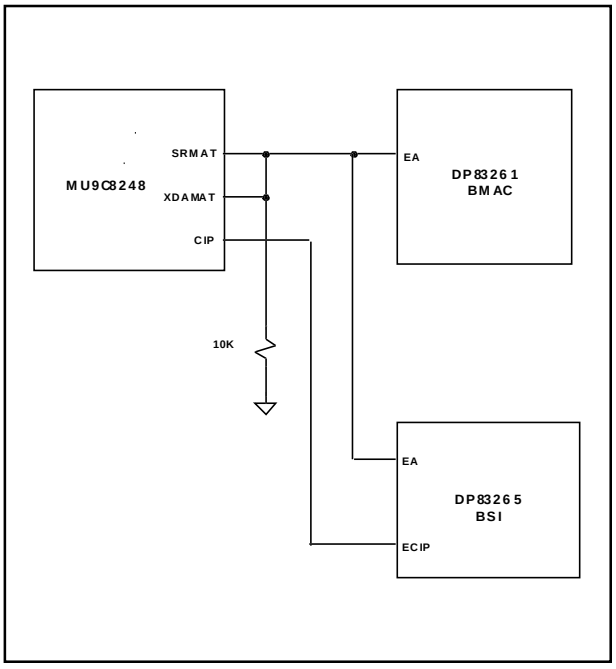


Figure 3: NS MAC/BSI Connection Diagram

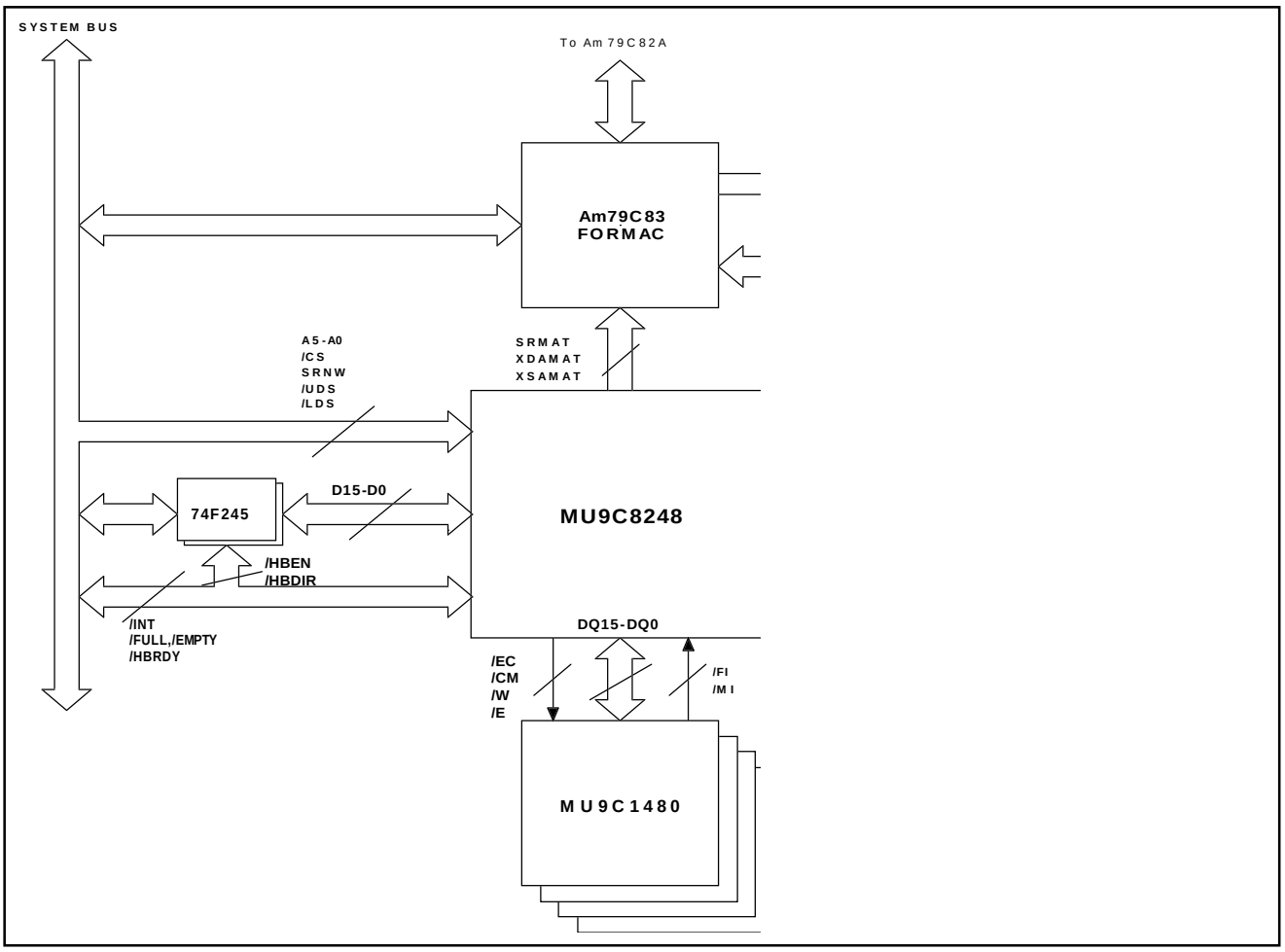


Figure 4: AMD Connection Diagram

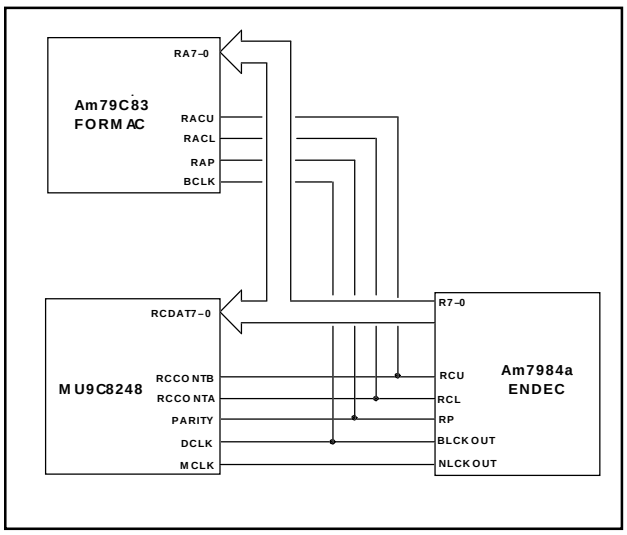


Figure 5: AMD Transceiver Connection Diagram

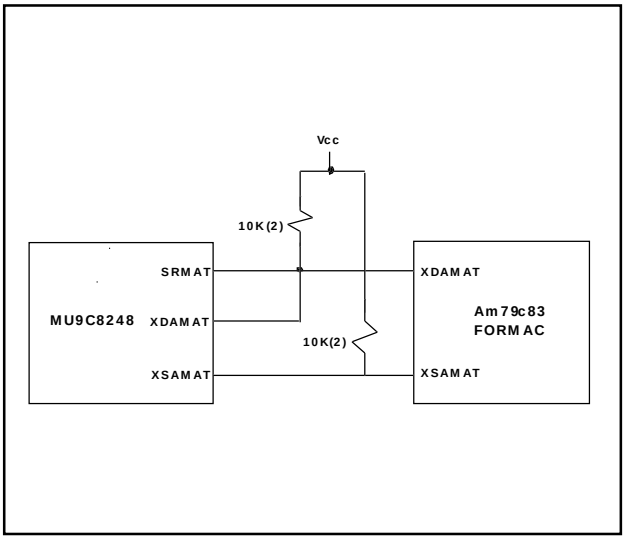


Figure 6: AMD MAC Connection Diagram

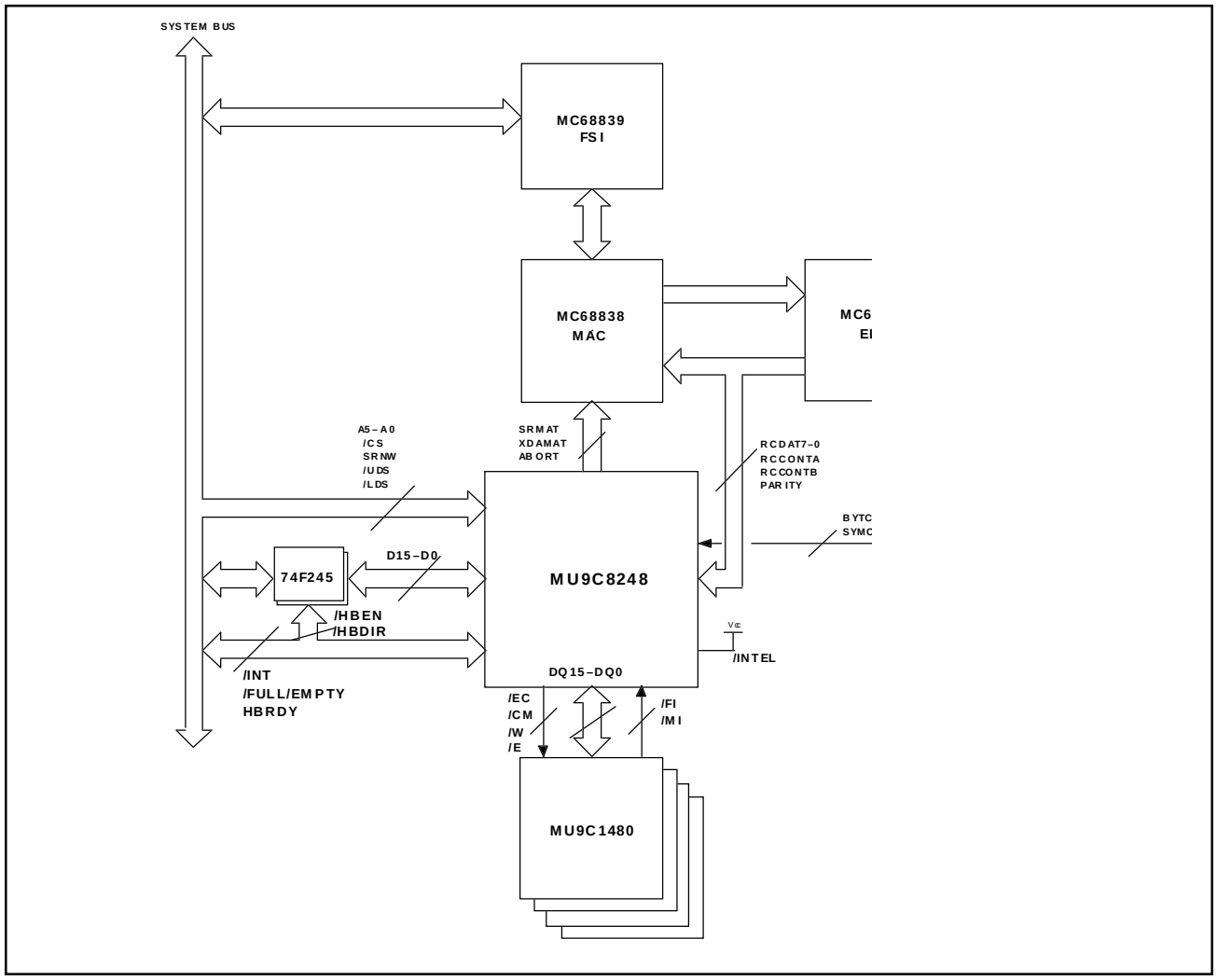


Figure 7: Motorola Connection Diagram

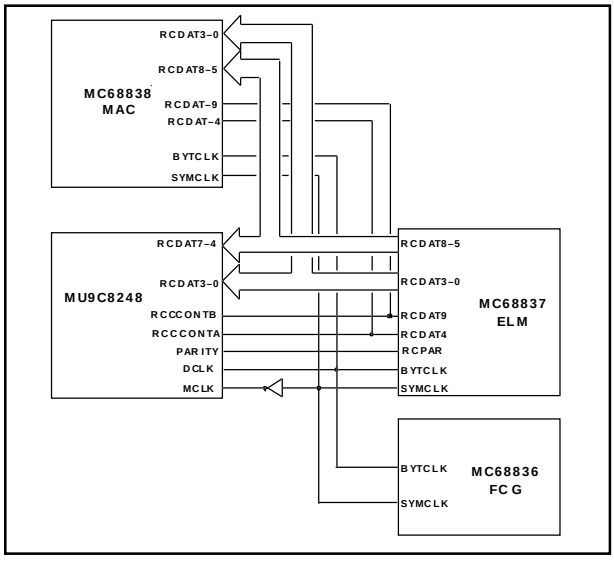


Figure 8: Motorola Transceiver Connection Diagram

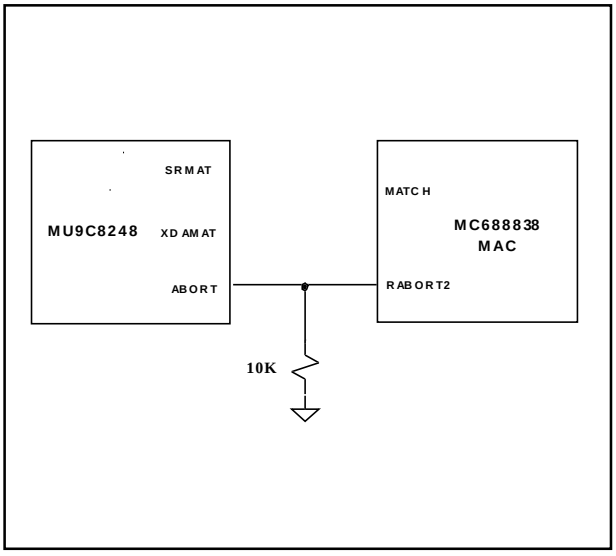


Figure 9: Motorola MAC Connection Diagram

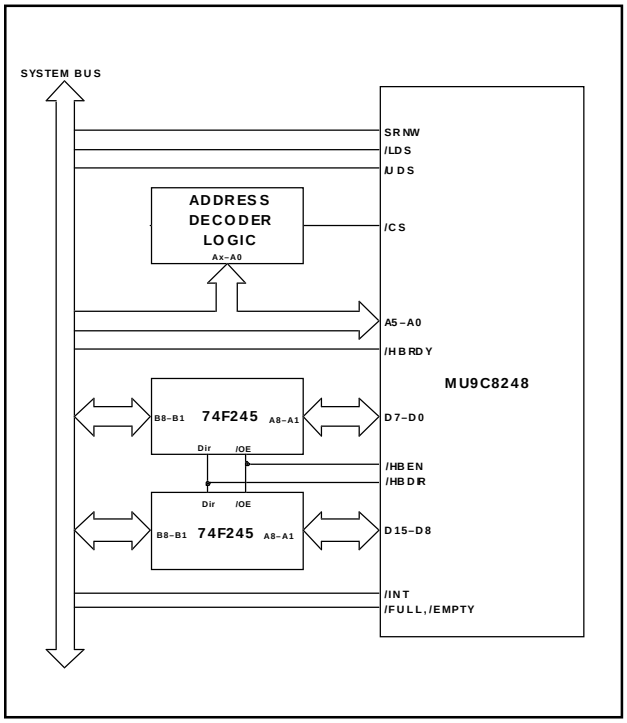


Figure 10: Motorola Connection Diagram

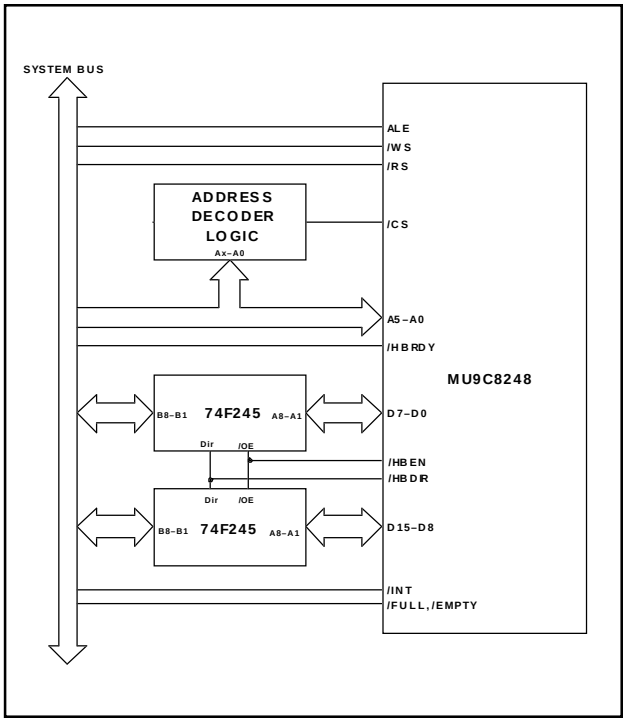


Figure 11: Intel Connection Diagram

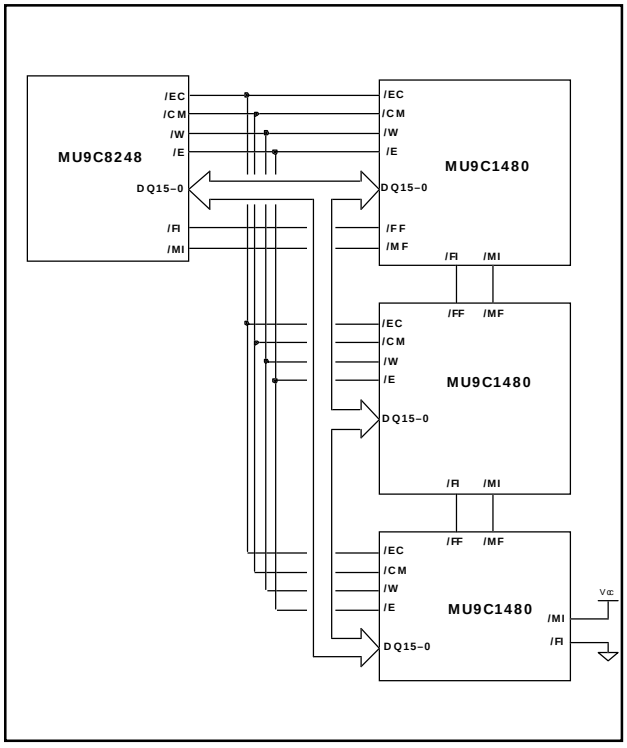


Figure 12: MU9C8148 Diagram

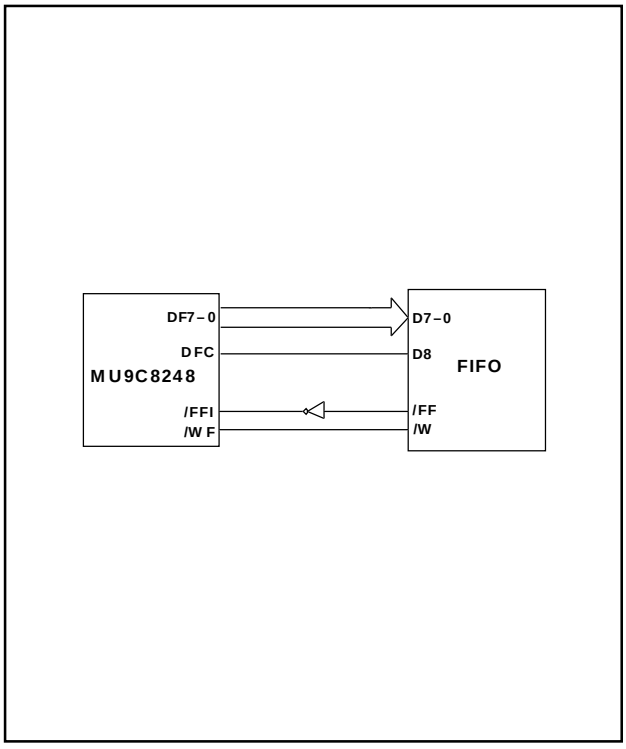


Figure 13: FIFO Connection Diagram

Before downloading the filtering routines and enabling the MU9C8248 filtering actions, the device should be initialized. An example MU9C8248 initialization routine looks like the following:

Register	Data	Comments
00H	8000H	Resets the MU9C8248
00H	2000H	NS Mode, SRT, Only learning SAs from error-free frames, Also learning SAs of frames which contain a RIF, Enable reception of STE frames, Set address pointer 00H
02H	74FFH	Negative filtering, Discard all BA, GA, FA, Only learn SAs from LLC frames, Polarity of the signals at the ED of the frame
03H	888AH	Every frame (SRF, ARE and STE) is rejected when the number of RDs >=8, XDAMAT and SRMAT are enabled
04H	0123H	The Source ring-number is 123H
05H	6456H	Destination ring-number is 456H and the associated bridge-number is 6H
06H	5789H	Destination ring-number is 789H and the associated bridge-number is 5H
07H	9076H	Destination ring-number is 076H and the associated bridge-number is 9H

LANCAM Initialization

This initialization routine is followed by a LANCAM initialization routine. In this specific example two LANCAMs are programmed via the MU9C8248. The initialization routine shown gives all registers an initial value.

Register	Data	Comments
24H	0000H	Accounts for Power-up anomalities
24H	0228H	TCO DS
24H	FFFFH	Disable device select feature
24H	0200H	TCO CT
24H	0000H	Reset LANCAM
24H	0208H	TCO PA
24H	0000H	Set first Page Address to 0000H
24H	0700H	SFF
24H	0208H	TCO PA
24H	0001H	Set second Page Address to 0001H
24H	0200H	TCO CT
24H	0000H	Causes Reset
24H	0210H	TCO SC
24H	1C04H	Set DCS=00,DCE=11,DC=00
24H	0110H	SPD MR2
26H	0000H	MR2 Value
26H	FFFFH	
26H	FFFFH	
26H	FFFFH	
24H	0005H	SPS_M@HM
24H	0100H	SPD CR

The MR2 register of the LANCAM is used by the "Purge on Associated Data" routine.

MU9C8248 Filtering Routines

The LANCAM initialization routine is followed by code sequences that program routines into the MU9C8248 Instruction buffer by writing into register 15H. The following code sequences are only examples, and will likely need to be optimized for the specific application. First, a DA/SA Comparison routine is written to this address, as typified by Routine 0 (Figure 14). The code listing shows where in memory this specific routine is stored. After Routine 0, an SA Learning routine is loaded, as typified by Routine 1 (Figure 15). Finally, a "Purge on Address" routine, as typified by Routine 2 (Figure 16), a "Purge on Associated Data" routine as typified by Routine 3 (Figure 17) and a "Download Time stamp" routine as typified by routine 4 (Figure 18) are loaded. The last thing to do is to enable the MU9C8248 to perform these routines on the FDDI data by writing:

16H	8E80H	Start address for Routine 0 is 00H, start address for Routine 1 is 0EH, enable routine 0 and 1
19H	0800H	Delay start routine 0 by 0 MCLK cycles, enable external FIFO
1EH	0404H	Enable LLC frame counter and data byte counter in LLC frames
01H	3030H	Enable SR and TB filtering on LLC frames

MU9C8248 Instructions

Instructions are written into the Instruction buffer in two Host processor write cycles for each 24-bit memory location: the first cycle loads a 16-bit LANCAM op-code or data, or MU9C8248 special instruction. The second cycle loads as the eight high-order bits (with the rest of the 16-bit word "don't cares") the state of the LANCAM control signals /W, /CM, /EC, the SP bit, which indicates LANCAM instruction vs. MU9C8248 instruction, the S bit which indicates that this instruction is the last instruction of this routine, and the L2-L0 bits which indicate the execution length of the instruction. /W, /CM, and /EC represent the controls for the LANCAM, and a full explanation of their operation is given in the MUSIC Semiconductors' LANCAM Handbook. When the MU9C8248 drives the LANCAM, the 16-bit op-code or data is placed on the DQ15–0 bus, and at the same time, the values stored for /W, /CM, and /EC are placed on their respective output lines to control the LANCAM operation. The /E enable signal for the LANCAM is generated by the MU9C8248. Table 1 shows the format of LANCAM instructions, as stored in the MU9C8248 Instruction buffer, and how the control bits stored in the second cycle are decoded to give the LANCAM control signals. Table 2 shows the special MU9C8248 instruction set, which is further explained in the MU9C8248 Datasheet. The second cycle values shown in Table 2 represent usual control signal levels for data transfer between the LANCAM and the MU9C8248.

DA/SA Comparison (Routine 0)

Routine 0, shown in Figure 14, is automatically started by the MU9C8248, and first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 48-bit CAM/16-bit RAM mode with no masking during comparison. The Segment Control register is then programmed to transfer three 16-bit segments of data containing either the Destination address or the Source address to the Comparand register. If no match on the DA is found, the frame will be accepted. If a match takes place, the frame will be discarded. The SA is placed in the Mask Register 1 together with a preloaded time stamp and the actual learning has to take place by Routine 1. SA Learning routine (Routine 1) will be started when no SA match took place and the frame was error free.

SA Learning (Routine 1)

Routine 1, shown in Figure 15, is automatically started by the MU9C8248, and first unlocks the LANCAM daisy chain and/or ends the previous instruction.

The SA to be learned was placed in Mask Register 1. Routine 1 moves the content of the MR1 to the next free location. At the same time a copy of the SA is placed in the external FIFO (see also Figure 13).

Purge on Address (Routine 2)

Routine 2, shown in Figure 16, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 48-bit CAM/16-bit RAM mode with no masking during comparison. The Segment Control register is programmed to transfer three 16-bit segments of data containing the address to purge to the Comparand register. If a matching address is found the validity bits of that location are set empty.

Routine 2 is started by the microcontroller by writing to the MU9C8248 Start register II; but first the address to be purged must be loaded into the databuffer as shown in the following instructions:

Register	Data	Comments
00H	2040H	Set address pointer to 40H (first location in data buffer)
15H	1234H	First part of the address
15H	0000H	Dummy cycle
15H	4567H	Second part of the address
15H	0000H	Dummy cycle
15H	1238H	Third part of the address
15H	0000H	Dummy cycle
17H	0090H	Start routine 2 immediately

First Cycle	Second Cycle	LANCAM Cycle Type
Op-Code or Register Value	0XXXH 2XXXH	Command Write, /EC=LOW Command Write, /EC=HIGH
Data to be Written	4XXXH 6XXXH	Data Write, /EC=LOW Data Write, /EC=HIGH
Register Value will be read out	8XXXH AXXXH	Command Read, /EC=LOW Command Read, /EC=HIGH
Data Value will be read out	CXXXH EXXXH	Data Read, /EC=LOW Data Read, /EC=HIGH

Table 1: Instruction Buffer Format for LANCAM Instructions

Purge on Associated Data (Routine 3)

Routine 3, shown in Figure 17, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 64-bit CAM mode with MR2 during comparison. The segment Control register is programmed to transfer 16 bits of data containing the time stamp to Segment 0 of the Comparand register. All matching addresses are emptied by setting the validity bits empty.

Routine 3 is started by the microcontroller by writing the MU9C8248 Start register II; but first the time stamp must be loaded:

Register	Data	Comments
00H	2043H	Set address pointer to 43H
15H	7456H	Time stamp
15H	0000H	Dummy cycle
17H	9A00H	Start Routine 3 immediately

Download Time stamp (Routine 4)

Routine 4, shown in Figure 18, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 64-bit CAM mode without masking during comparison. The Segment Control register is programmed to transfer 16 bits of data containing the new time stamp value to Segment 0 of the Comparand register.

First Cycle	Second Cycle	Desciption
2YAAH	FXXXH	Wait for match for Y+1 cycle, if no match then execute at AAH
3000H	7XXXH	Move data from DA part 0 to DQ15–0
3001H	7XXXH	Move data from DA part 1 to DQ15–0
3002H	5XXXH	Move data from DA part 2 to DQ15–0
3003H	7XXXH	Move data from SA part 0 to DQ15–0
3004H	7XXXH	Move data from SA part 1 to DQ15–0
30005H	5XXXH	Move data from SA part 2 to DQ15–0
4RAAH	7XXXH	Move data from AAH to DQ15–0
5RAAH	DXXXH	Move data from DQ15–0 to AAH
6RRRH	7XXXH	Move data from the FIFO to DQ15–0
7RRRH	DXXXH	Move data from DQ15–0 To the FIFO
	Notes:	"R" means Reserved Second Cycle values are typical

Table 2: MU9C8248 Instruction Set

Before starting Routine 4, the new time stamp has to be loaded into location 44H by the following routine:

Register	Data	Comments
00H	2044H	Set address pointer to 44H
15H	7345H	New time stamp
15H	0000H	Dummy cycle
18H	00A2H	Start Routine 4 immediately

PROGRAMMING EXAMPLES FOR THE MU9C8248

Second Example

In the second example the MU9C8248 is used in a SRT bridge on a port level, connected to a NS chipset. As in the first example, the port containing this interface is connected to ring number 123H, while three other ports of this bridge are connected to ring number 456H through bridge number 6H, ring number 789H through bridge number 5H, and ring number 076H through bridge number 9H. The difference between this example and the first example is that the MU9C8248 is set up to perform positive filtering with a LANCAM database size of 1k entries. An example of the MU9C8248 initialization routine could be:

Register	Data	Comments
00H	8000H	Resets the MU9C8248
00H	2000H	NS Mode, SRT, Only learning SAs from error-free frames, Also learning SAs of frames which contain a RIF, Enable reception of STE frames, Set address pointer 00H
02H	84FFH	Positive filtering, Only learn SAs from LLC frames, Polarity of the signals to the MAC is Active-HIGH, Deassertion of those signals at the ED of the frame
03H	888AH	Every frame (SRF, ARE and STE) is rejected when the number of RDs>=8, XDAMAT and SRMAT are enabled
04H	0123H	The Source ring-number is 123H
05H	6456H	Destination ring-number is 456H and the associated bridge-number is 6H
06H	5789H	Destination ring-number is 789H and the associated bridge-number is 5H
07H	9076H	Destination ring-number is 076H and the associated bridge-number is 9H

LANCAM Initialization

The initialization routine is followed by a LANCAM initialization routine. In this specific example LANCAM is programmed via the MU9C8248. The initialization routine shown gives all registers an initial value.

Register	Data	Comments
24H	0000H	Accounts for Power-up anomalities
24H	0228H	TCO DS
24H	FFFFH	Disable device select feature
24H	0200H	TCO CT
24H	0000H	Reset LANCAM
24H	0208H	TCO PA
24H	0000H	Set Page Address to 0000H
24H	0200H	TCO CT
24H	0000H	Causes Reset
24H	0210H	TCO SC
24H	1C04H	Set DCS=00,DCE=11,DC=00
24H	0110H	SPD MR2
26H	0000H	MR2 Value
26H	FFFFH	
26H	FFFFH	
26H	FFFFH	
24H	0005H	SPS_M@HM
24H	0100H	SPD CR

The MR2 register of the LANCAM is used by the “Purge on Associated Data” routine.

MU9C8248 Filtering Routines

The LANCAM initialization routine is followed by code sequences that program routines into the MU9C8248 Instruction buffer by writing into register 15H. The following code sequences are only examples, and will likely need to be optimized for the specific application. First, a DA/SA Comparison routine is written to this address, as typified by Routine 0 (Figure 19). The code listing shows where in memory this specific routine is stored. Routine 1, used as a network triggered learning routine is not used. Learning takes place by having each network port placing the SA of each frame into an FIFO (Figure 13). Each address in the FIFO is then checked against the addresses in the LANCAM databases of all the other ports of that bridge and if the address is not found in a specific LANCAM database, it is learned. This checking and learning is done by a Learning routine, as typified by Routine 2 (Figure 20) whereby addresses received from other network ports are used. Finally, a “Purge on Address” routine, as typified by Routine 3 (Figure 21), a “Purge on Associated Data” routine as typified by Routine 4 (Figure 22) and a “Download Time stamp” routine as typified by routine 5 (Figure 23) are loaded. The last thing to do is to enable the MU9C8248 to perform these routines on the FDDI data by writing:

Register	Data	Comments
16H	8000H	Start address for Routine 0 is 00H, enable routine 0
19H	0800H	Delay start routine 0 by 0 MCLK cycles, enable external FIFO
1EH	0404H	Enable LLC frame counter and data byte counter in LLC frames
01H	3030H	Enable SR and TB filtering on LLC frames

DA/SA Comparison (Routine 0)

Routine 0, shown in Figure 19, is automatically started by the MU9C8248, and first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 48-bit CAM/16-bit RAM mode with no masking during comparison. The Segment Control register is then programmed to transfer three 16-bit segments of data containing either the Destination address or the Source address to the Comparand register. If a match on the DA is found, the frame will be accepted. If no match takes place, the frame will be discarded. If the frame is error-free, the SA is always moved into the external FIFO because an SA match will never occur.

Learning (Routine 2)

Routine 2, shown in Figure 20, is a microcontroller triggered routine. It first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 48-bit CAM/16-bit RAM mode with no masking during comparison. The Segment Control register is programmed to transfer three 16-bit segments of data containing the address to learn to the Comparand register. If a matching address is found the address in the Comparand register is moved to that location thereby updating the time stamp of that specific address. If there is no matching location, the content of the Comparand register is moved into the next free address.

Routine 2 is started by the microcontroller by writing to the MU9C8248 Start register II; but first the address to be purged must be loaded into the databuffer as shown in the following instructions:

Register	Data	Comments
00H	2040H	Set address pointer to 40H (first location in data buffer)
15H	1234H	First part of the address
15H	0000H	Dummy cycle
15H	4567H	Second part of the address
15H	0000H	Dummy cycle
15H	1238H	Third part of the address
15H	0000H	Dummy cycle
17H	008CH	Start routine 2 immediately

Purge on Address (Routine 3)

Routine 3, shown in Figure 21, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 48-bit CAM/16-bit RAM mode with no masking during comparison. The Segment Control register is programmed to transfer three 16-bit segments of data containing the address to purge to the Comparand register. If a matching address is found the validity bits of that location are set empty.

Routine 3 is started by the microcontroller by writing to the MU9C8248 Start register II; but first the address to be purged must be loaded into the databuffer as shown in the following instructions:

Register	Data	Comments
00H	2043H	Set address pointer to 43H (first location in data buffer)
15H	1234H	First part of the address
15H	0000H	Dummy cycle
15H	4567H	Second part of the address
15H	0000H	Dummy cycle
15H	1238H	Third part of the address
15H	0000H	Dummy cycle
17H	9800H	Start routine 3 immediately

Purge on Associated Data (Routine 4)

Routine 4, shown in Figure 22, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 64-bit CAM mode with MR2 during comparison. The Segment Control register is programmed to transfer 16-bits of data containing the time stamp to Segment 0 of the Comparand register. All matching addresses are emptied by setting the validity bits empty.

Routine 4 is started by the microcontroller by writing to the MU9C8248 Start register III; but first the time stamp must be loaded:

Register	Data	Comments
00H	2046H	Set address pointer to 46H
15H	7456H	Time stamp
15H	0000H	Dummy cycle
18H	00A1H	Start Routine 4 immediately

Download Time stamp (Routine 5)

Routine 5, shown in Figure 23, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Control register programs the LANCAM in a 64-bit CAM mode without masking during comparison. The Segment Control register is programmed to transfer 16 bits of data containing the new time stamp value to Segment 0 of the Comparand register.

Before starting Routine 5, the new time stamp has to be loaded into location 47H by the following routine:

Register	Data	Comments
00H	2047H	Set address pointer to 47H
15H	7345H	New time stamp
15H	0000H	Dummy cycle
18H	A800H	Start Routine 5 immediately

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
00	0000 A000		Dummy Cycle - Clears Power previous cycle, Command Re
01	0000 A000		Dummy Cycle Command Read, /EC=HIGH,
02	0200 2000	TCO_CT	Target Control Register Command Write, /EC=HIGH,
03	8040 2000		48 CAM, 16 RAM, No Mask, Command Write, /EC=HIGH,
04	0210 2000	TCO_SC	Target Segment Control Regis Command Write, /EC=HIGH,
05	39C9 2000		Write to Segments 1-3, Read Command Write, /EC=HIGH,
06	0506 2100	CMP S	Compare “Skip” Locations (F Command Write, /EC=HIGH,
07	3002 7000		Move DA Part 2 to LANCAM Data Write, /EC=HIGH, /E=1
08	3001 7000		Move DA Part 1 to LANCAM Data Write, /EC=HIGH, /E=1
09	3000 5100		Move DA Part 0 to LANCAM Data Write, /EC=LOW, /E=2
0A	0506 2100	CMP S	Compare “Skip” Locations (F Command Write, /EC=HIGH,
0B	3005 7000		Move SA Part 2 to LANCAM Data Write, /EC=HIGH, /E=1
0C	3004 7000		Move SA Part 1 to LANCAM Data Write, /EC=HIGH, /E=1
0D	3003 5100		Move SA Part 0 to LANCAM Data Write, /EC=LOW, /E=2
0E	0328 2100	MOV HM, CR	Move to Memory @ Highest Command Write, /EC=HIGH,
0F	0308 2800	MOV MR1, CR	Move to Mask Register 1 fron Command Write, /EC=HIGH,
10	0300 A800	NOP	No Operation Command Read, /EC=HIGH,

Figure 14: DA/SA Comparison (Routine 0)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
11	0001 A000		Dummy Cycle Command Read,
12	0001 A000		Dummy Cycle Command Read,
13	0335 2900	MOV_NF, MR1 V	Move to Next Free Command Write,
14	0300 A800	NOP	No Operation Command Write,

Figure 15: SA Learning (Routine 1)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
15	0002 A000		Dummy Cycle Command Read, /EC=H
16	0200 2000	TCO_CT	Target Control Register Command Write, /EC=H
17	8040 2000		48 CAM, 16 RAM, No M Command Write, /EC=H
18	0210 2000	TCO_SC	Target Segment Contro Command Write, /EC=H
19	39C9 2000		Write to Segments 1-3, Command Write, /EC=H
1A	4040 7000		Move data from SRT Ac Data Write, /EC=HIGH,
1B	4041 7000		Move data from SRT Ac Data Write, /EC=HIGH,
1C	4042 5100		Move data from SRT Ac Data Write, /EC=LOW,
1D	0300 2000	NOP	No Operation Command Write, /EC=H
1E	042D 2900	VBC HM, E	Set Validity Bits at High Command Write, /EC=H
1F	0300 A800	NOP	No Operation Command Write, /EC=H

Figure 16: Purge on Address (Routine 2)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
20	0003 A000		Dummy Cycle Command Read, /EC=H
21	0200 2000	TCO_CT	Target Control Register Command Write, /EC=H
22	8020 2000		64 CAM, 0 RAM, Mask Command Write, /EC=H
23	0210 2000	TCO_SC	Target Segment Contro Command Write, /EC=H
24	0404 2000		Write to Segment 0, Re Command Write, /EC=H
25	4043 5100		Move data from SRT Ac Data Write, /EC=LOW,
26	0300 2000	NOP	No Operation Command Write, /EC=H
27	043D 2900	VBC ALM, E	Set Validity Bits at High Command Write, /EC=H
28	0300 A800	NOP	No Operation Command Write, /EC=H

Figure 17: Purge on Associated Data (Routine 3)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
29	0004 A000		Dummy Cycle Command Read, /E
2A	0200 2000	TCO_CT	Target Control Reg Command Write, /E
2B	8020 2000		64 CAM, 0 RAM, M Command Write, /E
2C	0210 2000	TCO_SC	Target Segment C Command Write, /E
2D	0404 2000		Write to Segment (Command Write, /E
2E	4044 7800		Move data from SF Data Write, /EC=H
2F	0300 A800	NOP	No Operation Command Write, /E

Figure 18: Downloading Timestamp (Routine 4)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
00	0000 A000		Dummy Cycle - Clears Power- complete previous cycle, Comr
01	0000 A000		Dummy Cycle Command Read, /EC=HIGH, /E
02	0200 2000	TCO_CT	Target Control Register Command Write, /EC=HIGH, S
03	8040 2000		48 CAM, 16 RAM, No Mask, In Command Write, /EC=HIGH, /E
04	0210 2000	TCO_SC	Target Segment Control Regist Command Write, /EC=HIGH, /E
05	39C9 2000		Write to Segments 1-3, Read fr Command Write, /EC=HIGH, /E
06	0506 2100	CMP S	Compare “Skip” Locations (For Command Write, /EC=HIGH, /E
07	3002 7000		Move DA Part 2 to LANCAM Data Write, /EC=HIGH, /E=1 M
08	3001 7000		Move DA Part 1 to LANCAM Data Write, /EC=HIGH, /E=1 M
09	3000 5200		Move DA Part 0 to LANCAM Data Write, /EC=LOW, /E=3 M
0A	0300 A000	NOP	No Operation Command Read, /EC=HIGH, /E
0B	0506 2100	CMP S	Compare “Skip” Locations (For Command Write, /EC=HIGH, /E
0C	3005 7000		Move SA Part 2 to LANCAM Data Write, /EC=HIGH, /E=1 M
0D	3004 7000		Move SA Part 1 to LANCAM Data Write, /EC=HIGH, /E=1 M
0E	3003 5A00		Move SA Part 0 to LANCAM Data Write, /EC=LOW, /E=3 M
0F	0300 A000	NOP	No Operation Command Read, /EC=HIGH /E

Figure 19: DA/SA Comparison (Routine 0)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
10	0002 A000		Dummy Cycle Command Read, /EC=HIGH, /E
11	0200 2000	TCO_CT	Target Control Register Command Write, /EC=HIGH, /E
12	8040 2000		48 CAM, 16 RAM, No Mask, In Command Write, /EC=HIGH, /E
13	0210 2000	TCO_SC	Target Segment Control Regist Command Write, /EC=HIGH, /E
14	39C9 2000		Write to Segments 1-3, Read fr Command Write, /EC=HIGH, /E
15	4040 7000		Move data from SRT Address 4 Data Write, /EC=HIGH, /E=1 M
16	4041 7000		Move data from SRT Address 4 Data Write, /EC=HIGH, /E=1 M
17	4042 5200		Move data from SRT Address 4 Data Write, /EC=LOW, /E=3 M
18	2016 1000		Wait 5 cycles for Match; If No M 1 MCLK Cycle
19	0328 2A00	MOV HM, CR	Move to Memory @ Highest Ma Command Write, /EC=HIGH, /E
1A	0300 2000	NOP	No Operation Command Write, /EC=HIGH, /E
1B	0334 2A00	MOV_NF, CR V	Move to Next Free address fron Command Write, /EC=HIGH, /E
1C	0300 A000	NOP	No Operation Command Read, /EC=HIGH /E

Figure 20: Learning (Routine 2)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
1D	0003 A000		Dummy Cycle Command Read, /EC=HIGH, /E
1E	0200 2000	TCO_CT	Target Control Register Command Write, /EC=HIGH, /E
1F	8040 2000		48 CAM, 16 RAM, No Mask, In Command Write, /EC=HIGH, /E
20	0210 2000	TCO_SC	Target Segment Control Regist Command Write, /EC=HIGH, /E
21	39C9 2000		Write to Segments 1-3, Read fr Command Write, /EC=HIGH, /E
22	4043 7000		Move data from SRT Address 4 Data Write, /EC=HIGH, /E=1 M
23	4044 7000		Move data from SRT Address 4 Data Write, /EC=HIGH, /E=1 M
24	4045 5200		Move data from SRT Address 4 Data Write, /EC=LOW, /E=3 M
25	042D 2900	VBC HM, E	Set Validity bits at Highest Mat Command Write, /EC=HIGH, /E
26	0300 A000	NOP	No Operation Command Read, /EC=HIGH /E

Figure 21: Purge on Address (Routine 3)

Address (HEX)	Data 31-0 (HEX)	Mnemonic	
27	0004 A000		Dummy Cycle Command Read, /EC=HIGH, /E
28	0200 2000	TCO_CT	Target Control Register Command Write, /EC=HIGH, /E
29	8020 2000		64 CAM, 0 RAM, MR2, Increm Command Write, /EC=HIGH, /E
2A	0210 2000	TCO_SC	Target Segment Control Regist Command Write, /EC=HIGH, /E
2B	0404 2000		Write to Segment 0, Read from Command Write, /EC=HIGH, /E
2C	4046 5200		Move data from SRT Address 4 Data Write, /EC=LOW, /E=3 M
2D	043D 2900	VBC ALM, E	Set Validity bits of All Matching Command Write, /EC=HIGH, /E
2E	0300 A000	NOP	No Operation Command Read, /EC=HIGH /E

Figure 22: Purge on Associated Data (Routine 4)

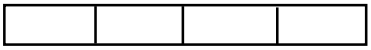
Address (HEX)	Data 31-0 (HEX)	Mnemonic	
2F	0005 A000		Dummy Cycle Command Read, /EC=HIGH, /E
30	0200 2000	TCO_CT	Target Control Register Command Write, /EC=HIGH, /E
31	8020 2000		64 CAM, 0 RAM, MR2, Increm Command Write, /EC=HIGH, /E
32	0210 2000	TCO_SC	Target Segment Control Regist Command Write, /EC=HIGH, /E
33	0404 2000		Write to Segment 0, Read from Command Write, /EC=HIGH, /E
34	4047 5200		Move data from SRT Address 4 Data Write, /EC=LOW, /E=3 M
35	0300 A000	NOP	No Operation Command Read, /EC=HIGH /E

Figure 23: Download Timestamp (Routine 5)

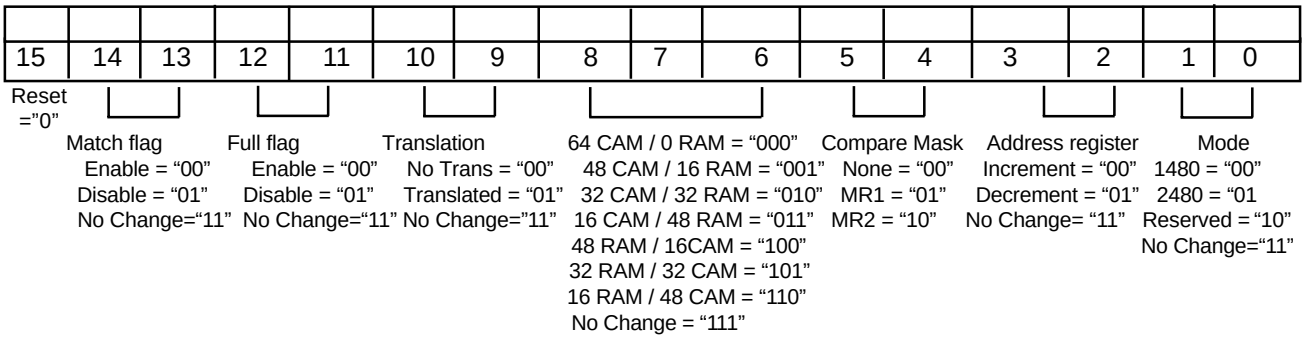
SRT Rountine Worksheet

Address (HEX)	Data 31-0 (HEX)	Mnemonic	

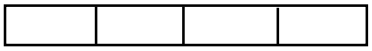
CAM Worksheet



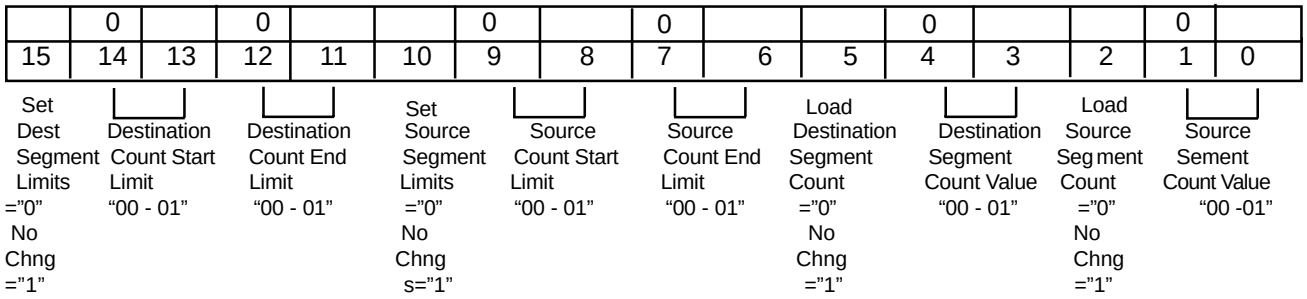
Hex Value



Control Register Bit Assignments



Hex Value



Segment Control Register Bit Assignments

NOTES

NOTES

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