MUSIC SEMICONDUCTORS

APPLICATION NOTE
AN - N4

USING THE MU9C8148 SRT INTERFACE

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INTRODUCTION

The MUSIC Semiconductors' MU9C8148 Source Routing Transparent interface accelerates Token Ring bridges and brouters when used with the MUSIC MU9C1480 LANCAM, provides a complete Source Routing Transparent filtering solution for Texas Instruments' Token Ring chipset, and increases bridge (brouter) performance with lowered system costs.

The MU9C8148 permits Source routing over multiple ports for full-mesh architectures, as well as the virtual ring concept. It provides for various validity checks on the Source routing information contained in the Routing Information Field (RIF), thereby freeing valuable processor time. To give basic support for network management, the MU9C8148 keeps track of errors in the RIF and totals them in error counters for statistical purposes.

The MU9C8148 parses the Token Ring frames to determine whether Source routing or Transparent bridging is being used, filters the Source Routed address fields, controls the MUSIC MU9C1480 LANCAM(s) for Transparent address filtering, and reports the results of the address comparisons to the Token Ring chipsets, "glue-free." User-definable program routines, such as comparing and learning, are stored in the MU9C8148, and do not need any direct microprocessor intervention.

This Application note outlines how to apply the MU9C8148 from a hardware point of view, and gives some example routines useful for Transparent bridging, supplementing the information provided in the MU9C8148 Datasheet.

CONNECTION DIAGRAMS

The MU9C8148 Connected to the TI Token Ring Chipset

In Figure 1, the MU9C8148 is connected to the Texas Instruments' TMS380CX6 MAC controller and the TMS38053/4 transceiver, and monitors the Transceiver output data from the network, as shown in Figure 2. The MU9C8148 generates XMATCH and XFAIL signals to tell the TMS380CX6 MAC controller chip to copy or discard a frame, as shown In Figure 3. The outputs of the MU9C8148 are high impedance when they are not active, to permit additional external address compare circuits, if desired. Since these lines are Active-HIGH, they both need a pull down resistor.

The MU9C8148 Controlled by a Motorola Microcontroller

The MU9C8148 can be controlled by a Motorola Microcontroller when used in the Motorola addressing mode, by tying the input pin /INTEL HIGH. Signals SRNW, /LDS, and /UDS define the read and write cycles to MU9C8148 registers. A4–A0 and /CS determine which register of the MU9C8148 is accessed. The databus can be buffered by two 74F245 bi-directional buffers, which are then controlled by the /HBEN and /HBDIR signals from the MU9C8148. If the MU9C8148 needs more time for a register access, the MU9C8148 automatically stretches the microcontroller cycle by delaying /HBRDY. Outputs /INT, /FULL, and /EMPTY can be used by the microcontroller system to schedule the accesses to the MU9C8148. A detailed connection diagram to the Motorola environment is shown in Figure 7.

The MU9C8148 Controlled by an Intel Microcontroller

The connection of the MU9C8148 to an Intel environment or a Motorola environment only differs for the signals that indicate the microcontroller cycle. In the case of an Intel environment, the /INTEL pin is grounded, and the ALE, /RS and /WS signals determine the microcontroller cycle. All the other signals as described for the Motorola environment keep their functionality as mentioned. A detailed connection to the Intel environment is shown in Figure 8.

The MU9C8148 Connected to the MU9C1480 LANCAM

The MU9C8148 uses the MU9C1480(s) to do the address compare necessary for Transparent bridging. The MU9C8148 provides all the control needed for the LANCAM interface in either a single LANCAM or multiple LANCAM configuration, as shown in Figure 9. No additional components are needed to couple the devices.

When the LANCAMs are shared by two MU9C8148s, the situation is more complex. Each MU9C8148 takes its output signals to the LANCAMs to HIGH-Z when it has finished its access to the LANCAMs. Thus, pull-up resistors are needed on all the control lines to prevent ambiguity. Built-in arbitration keeps the two MU9C8148s from interfering with each other, as shown in Figure 10.

PROGRAMMING EXAMPLES FOR THE MU9C8148

MU9C8148 Initialization

For the following example, the MU9C8148 is used in an SRT bridge on a port level, using the Texas Instruments chipset. For the sake of this example, the port containing this interface is connected to ring number 123H, while three other ports of this bridge are connected to ring number 456H through bridge number 6H, ring number 789H through bridge number 5H, and ring number 076H through bridge number 9H. The MU9C8148 is set up to perform negative filtering.

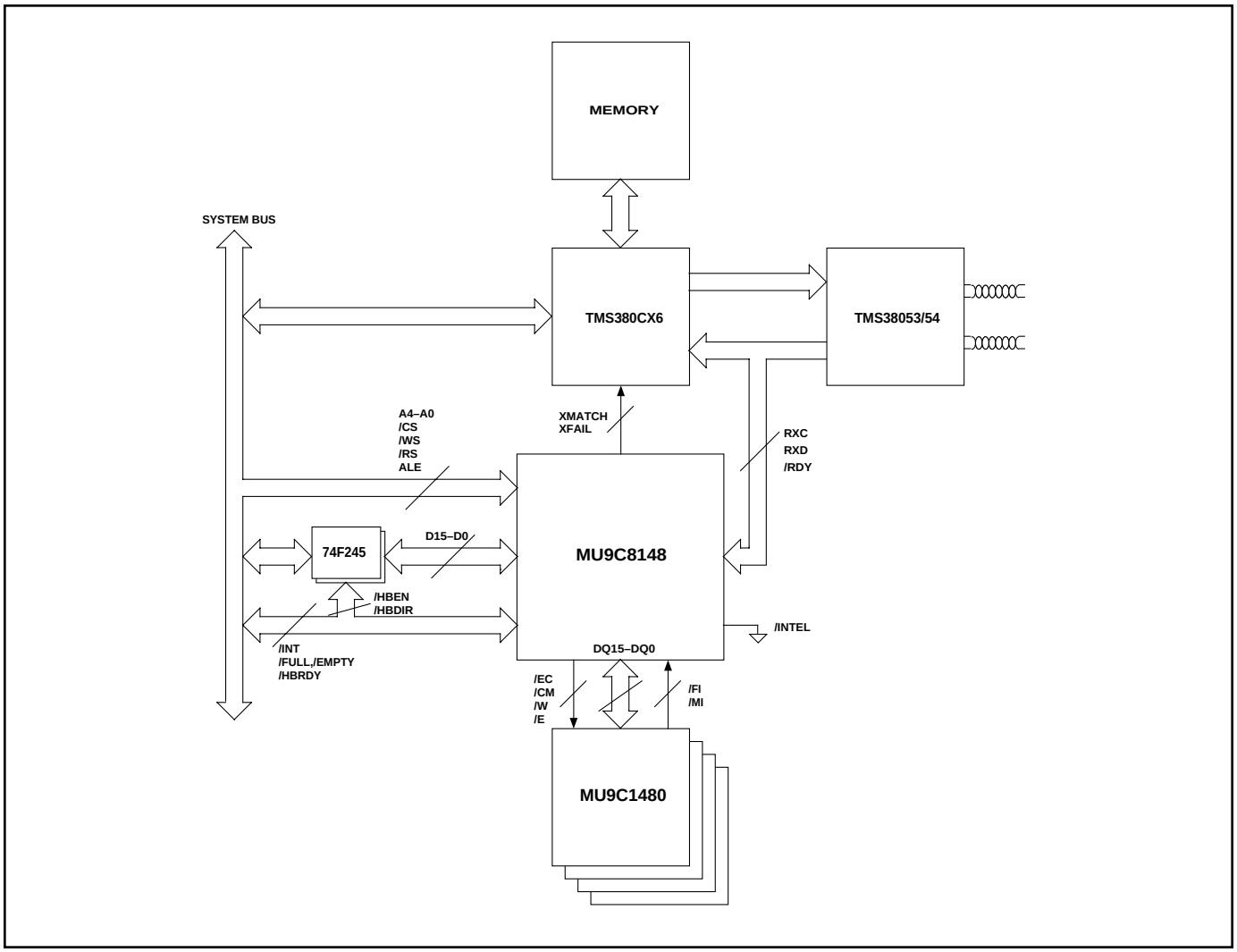

Figure 1: Texas Instruments Connection Diagram

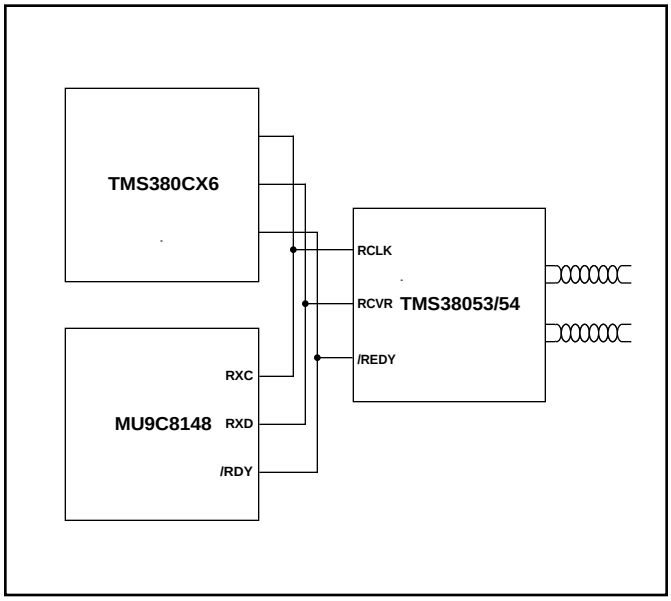

Figure 2: TI Transceiver Connection Diagram

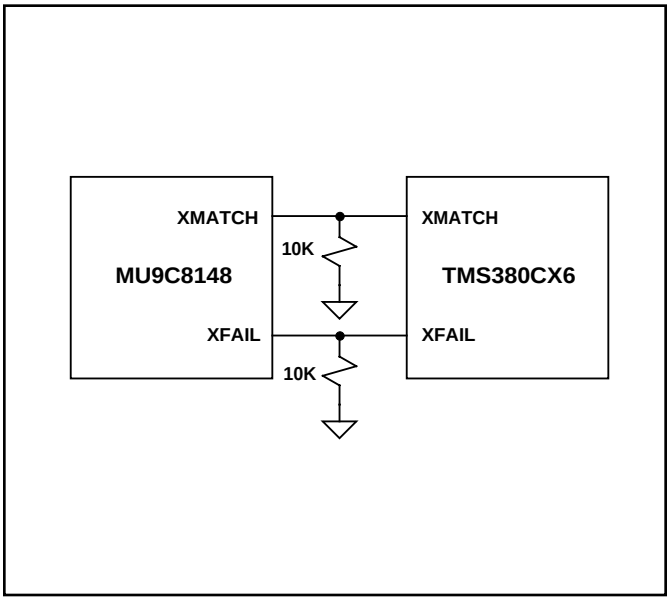

Figure 3: TI MAC Connection Diagram

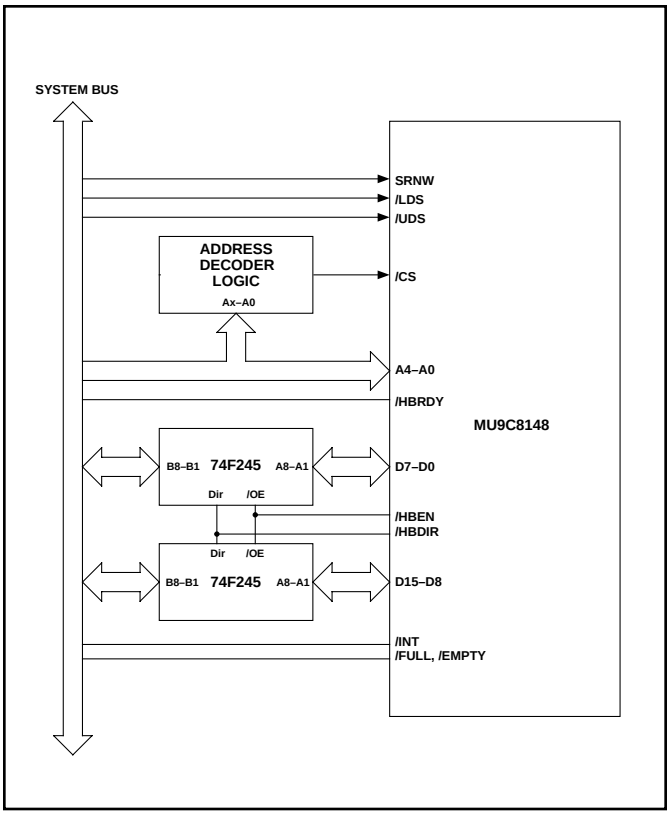

Figure 7: Motorola Connection Diagram

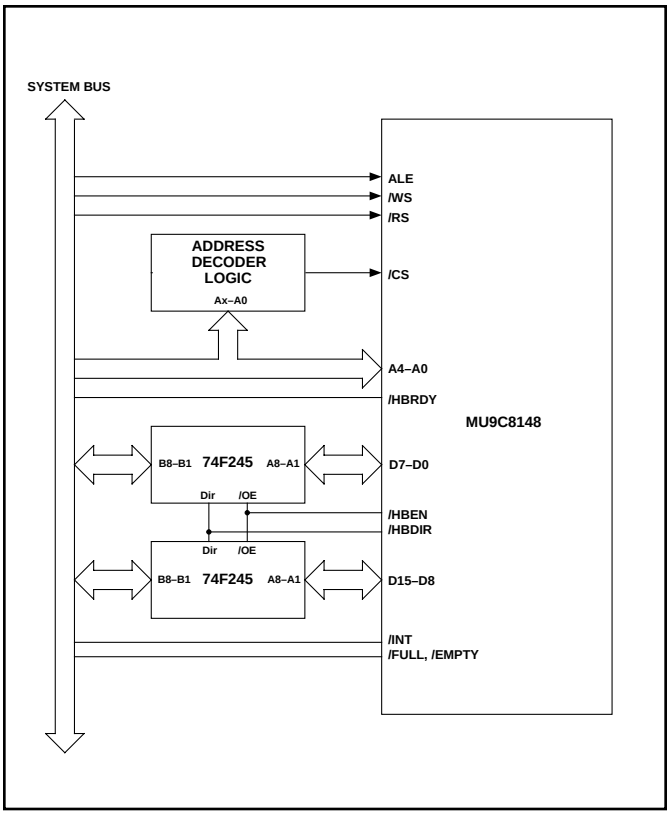

Figure 8: Intel Connection Diagram

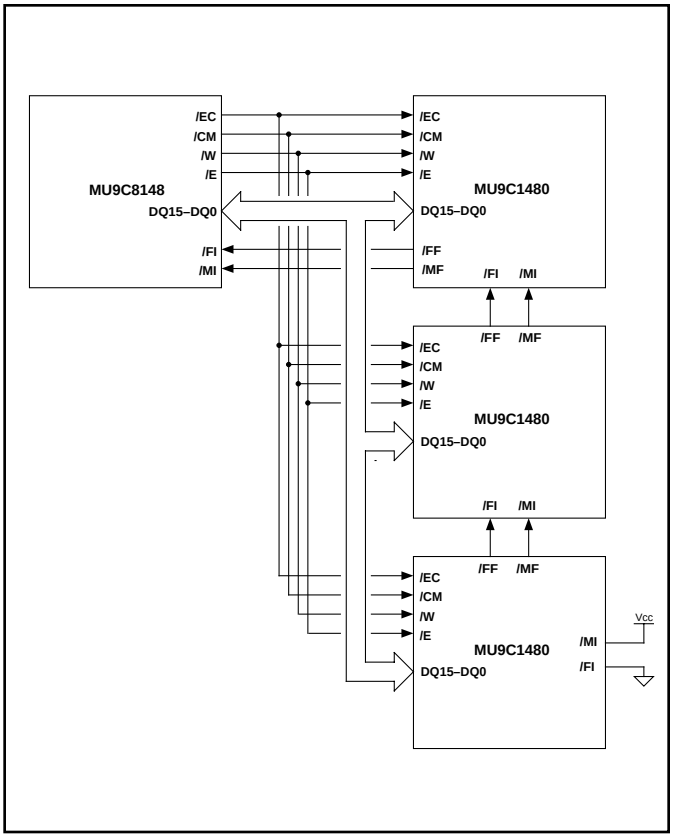

Figure 9: Single MU9C8148 Diagram

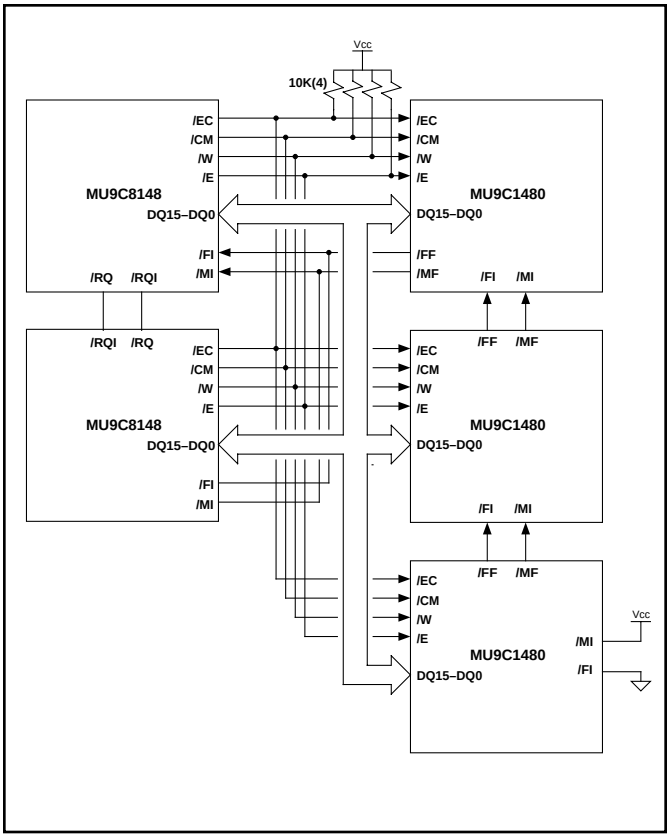

Figure 10: Dual MU9C8148 Diagram

Before enabling the MU9C8148 filtering actions, the device should be initialized. An example MU9C8148 initialization routine looks like the following:

Register	Data	Comments
00H	8000H	Resets the MU9C8148
00H	4000H	Texas Mode, SRT, Enable reception of STE frames, Set address pointer 00H
01H	3030H	Enable SR and TB filtering on LLC frames
03H	2108H	Every frame (SRF, ARE and STE) is rejected when the number of RDs >= 8
04H	0123H	The Source ring-number is 123H
05H	6456H	Destination ring-number is 456H and the associated bridge-number is 6H
06H	5789H	Destination ring-number is 789H and the associated bridge-number is 5H
07H	9076H	Destination ring-number is 076H and the associated bridge-number is 9H
0FH	0C00H	Start address for Routine 0 is 00H, start address for Routine 1 is 0CH
10H	3226H	Start address for Routine 2 is 26H, start address for Routine 3 is 32H
11H	003EH	Start address for Routine 4 is 3EH
12H	044CH	Enable FIFO, set flag on /EMPTY, lower limit is 4CH

LANCAM Initialization

This initialization routine is followed by a LANCAM initialization routine. All LANCAM(s) are programmed via the MU9C8148. The initialization routine shown sets the LANCAM as a 64-bit CAM, all registers are given an initial value, and the first two addresses in the LANCAM contain masks that are used by the routines run by the MU9C8148.

Register	Data	Comments
1CH	0000H	Accounts for Power-up anomalities
1CH	0228H	TCO DS
1CH	FFFFH	Disable device select feature
1CH	0200H	TCO CT
1CH	0000H	Reset LANCAM
1CH	0208H	TCO PA
1CH	0000H	Set Page Address to 0000H
1CH	0200H	TCO CT
1CH	8010H	Set Control Register initial values
1CH	0000H	SPS CR
1CH	0108H	SPD MR1
1CH	0210H	TCO SC
1CH	18C0H	Set Segment Control register initial values
1EH	7FFFH	First Mask Value
1EH	0000H	
1EH	0000H	
1EH	0000H	
1CH	0335H	MOV NF,MR1,V
1EH	0000H	Second Mask Value
1EH	FFFFH	
1EH	FFFFH	
1EH	FFFFH	
1CH	0335H	MOV NF,MR1,V
1CH	0427H	VBC [AR],R
1CH	0427H	VBC [AR],R

The CAM in the LANCAM is used in 64-bit CAM mode. The associated data is stored in Segment 0. The MSB of this associated data indicates whether an address is permanent (a bridge MAC address used for management purposes and filtered only by Routine 2) in which case it is set to ONE, or whether this address is dynamic and can be removed by the purge routines (MSB bit set to ZERO). The other bits of this associated data field are used as a time stamp. The specific masks that are necessary for this action are stored in memory addresses 000H and 001H, which are set to RAM-only, removing them from any compare cycles.

MU9C8148 Filtering Routines

The LANCAM initialization routine is followed by code sequences that program routines into the MU9C8148 Instruction buffer by writing into register 0CH. The following code sequences are only examples, and will likely need to be optimized for the specific application. First, a DA Comparison routine for dynamic entries is written to this address, as typified by Routine 0 (Figure 11). The code listing shows where in memory this specific routine is stored. After Routine 0, an SA Comparison routine is loaded, as typified by Routine 1 (Figure 12) and then a DA Comparison routine for permanent entries is loaded as typified by Routine 2 (Figure 13). Finally, a “Purge on Address” routine, as typified by Routine 3 (Figure 14) and a “Purge on Associated Data” routine as typified by Routine 4 (Figure 15) are loaded. The last thing to do is to enable the MU9C8148 to perform these routines on the Token Ring data by writing:

Register	Data	Comments
02H	040FH	Set negative filtering, Enable Routines 0,1,2 and enable learning on LLC frames

MU9C8148 Instructions

Instructions are written into the Instruction buffer in two Host processor write cycles for each 20-bit memory location: the first cycle loads a 16-bit LANCAM op-code or data, or MU9C8148 special instruction. The second cycle loads as the high-order nibble (with the rest of the 16-bit word “don’t cares”) the state of the LANCAM control signals /W, /CM, /EC, and the S bit, which indicates LANCAM instruction vs. MU9C8148 instruction. If the S bit is “0,” the nibble is “even,” and the instruction is for the LANCAM. If the S bit is “1,” the nibble is “odd,” and the instruction is for the MU9C8148. /W, /CM, and /EC repesent the controls for the LANCAM, and a full explanation of their operation is given in the MUSIC Semiconductors’ LANCAM Handbook. When the MU9C8148 drives the LANCAM, the 16-bit op-code or data is placed on the DQ15–DQ0 bus, and at the same time, the values stored for /W, /CM, and /EC are placed on their respective output lines to control the LANCAM operation. The /E enable signal for the LANCAM is generated by the MU9C8148. Table 1 shows the format of LANCAM instructions, as stored in the MU9C8148 Instruction buffer, and how the control bits stored in the second cycle are decoded to give the LANCAM control signals. Table 2 shows the special MU9C8148 instruction set, which is further explained in the MU9C8148 Datasheet. The second cycle values shown in Table 2 represent usual control signal levels for data transfer between the LANCAM and the MU9C8148.

First Cycle	Second Cycle	LANCAM Cycle Type
Op-Code or Register Value	0XXXH 2XXXH	Command Write, /EC=LOW Command Write, /EC=HIGH
Data to be Written	4XXXH 6XXXH	Data Write, /EC=LOW Data Write, /EC=HIGH
Register Value will be Read Out	8XXXH AXXXH	Command Read, /EC=LOW Command Read, /EC=HIGH
Data Value will be Read Out	CXXXH EXXXH	Data Read, /EC=LOW Data Read, /EC=HIGH

Table 1: Instruction Buffer Format for LANCAM Instructions

DA Comparison (Routine 0)

Routine 0, shown in Figure 11, is automatically started by the MU9C8148, and first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Segment Control register is then programmed to transfer four 16-bit segments of data containing the Destination address and associated data to the Comparand register. A mask is used to compare only the MSB of the associated data, which is set to a "0," and the Destination address with all the pre-stored dynamic addresses. This is accomplished by loading Mask register 1 with the data from memory address 000H. If no match is found, the frame will be accepted. If a match takes place, the frame will be discarded.

SA Comparison (Routine 1)

Routine 1, shown in Figure 12, is automatically started by the MU9C8148, and first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Segment Control register is programmed to transfer four 16-bit segments of data containing the Source address and associated data pre-stored in address 47H to the Comparand register. The Segment Control register is programmed so that the Source address and associated data can be read out from the LANCAM again.

Mask Register 1 is again used to compare only the MSB of the associated data and the Source address with all the pre-stored dynamic addresses. If no match is found, the Source address is learned by placing it in the next free location in the LANCAM, and the FIFO of the MU9C8148 is filled with the associated data and the Source address. This information can be used to update a general database. Routine 1 can be disabled by the Host Processor to stop learning of addresses.

If a match is found, the Source address is already in the database, and only needs an update of its time stamp. This new time stamp together with the Source address are placed in the FIFO ready to update the general database. The time stamp can be loaded into location 47H by the following routine:

First Cycle	Second Cycle	Description
0000H	FXXXH	Stop Execution
1YRRH	FXXXH	Wait for match for Y+3 cycles, if no match then execute at Branch Routine Address
2YAAH	FXXXH	Wait for match for Y+3 cycles, if no match then execute at AAH
3000H	7XXXH	Move data from DA part 0 to DQ15–DQ0
3001H	7XXXH	Move data from DA part 1 to DQ15–DQ0
3002H	5XXXH	Move data from DA part 2 to DQ15–DQ0
3003H	7XXXH	Move data from SA part 0 to DQ15–DQ0
3004H	7XXXH	Move data from SA part 1 to DQ15–DQ0
3005H	5XXXH	Move data from SA part 2 to DQ15–DQ0
4RAAH	7XXXH	Move data from AAH to DQ15–DQ0
5RAAH	DXXXH	Move data from DQ15–DQ0 to AAH
6RRRH	7XXXH	Move data from the FIFO to DQ15–DQ0
7RRRH	DXXXH	Move data from DQ15–DQ0 to the FIFO
	Notes:	"R" means Reserved Second Cycle values are typical

Table 2: MU9C8148 Instruction Set

Register	Data	Comments
00H	4047H	Set address pointer to 47H
0CH	7345H	Time stamp
0CH	0000H	

DA Comparison (Routine 2)

Routine 2, shown in Figure 13, is automatically started by the MU9C8148, and first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Segment Control register is programmed to transfer four 16-bit segments of data containing the Destination address and associated data to the Comparand register. A mask is used to compare only the MSB of the associated data, which is now set to a "1," and the Destination address with all the pre-stored permanent addresses. This is accomplished by loading Mask register 1 with the data from memory address 000H. If a match is found, the frame will be accepted. If no match is found, the frame will be discarded.

Purge on Address (Routine 3)

Routine 3, shown in Figure 14, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Segment Control register is programmed to transfer four 16-bit segments of data containing the Destination address and associated data to the Comparand register. Mask Register 1 is again used to compare only the MSB of the associated data and the Destination address with all the pre-stored dynamic addresses. This is accomplished by loading Mask register 1 with the data from memory address 000H. This compare cycle in the routine always finds a match. The matching address is then emptied.

Routine 3 is started by the microcontroller by writing to the MU9C8148 start register; but first, the address to be purged must be loaded as shown in the following instructions:

Register	Data	Comments
00H	4048H	Set address pointer to 48H
0CH	1234H	First part of the address
0CH	0000H	
0CH	4567H	Second part of the address
0CH	0000H	
0CH	1238H	Third part of the address
0CH	0000H	
0EH	4000H	Start routine 3 immediately

Purge on Associated Data (Routine 4)

Routine 4, shown in Figure 15, first unlocks the LANCAM daisy chain and/or ends the previous instruction. The Segment Control register is programmed to transfer 16 bits of data containing the time stamp to Segment 0 of the Comparand register. A mask is used to compare all the pre-stored dynamic addresses with only Segment 0 of the Comparand register (the MSB of the time stamp loaded in address 4BH should be ZERO). This is accomplished by loading Mask register 1 with the data from memory address 001H. All matching addresses are emptied.

Routine 4 is started by the microcontroller by writing to the MU9C8148 start register; but first, the time stamp must be loaded:

Register	Data	Comments
00H	404BH	Set address pointer to 4BH
0CH	7456H	Time stamp
0CH	0000H	
0EH	0400H	Start Routine 4 immediately

Address	Data	Comments
00H	0300	NOP
00H	2000	CW, /EC=HIGH UNLOCK DAISY CHAIN, AND/OR COMPLETE PREVIOUS INSTRUCTION
01H	0210	TCO SC
01H	2000	CW, /EC=HIGH
02H	18C0	DCS=00, DCE=11, DSC=00
02H	2000	CW, /EC=HIGH
03H	0100	SPD CR
03H	2000	CW, /EC=HIGH
04H	0B0C	MOVE MR1, AAAH
04H	2000	CW, /EC=HIGH
05H	0000	CAM ADDRESS 000H
05H	2000	CW, /EC=HIGH
06H	0000	0000H
06H	6000	DW, /EC=HIGH
07H	3000	MOVE DA PART 0 TO LANCAM
07H	7000	DW, /EC=HIGH
08H	3001	MOVE DA PART 1 TO LANCAM
08H	7000	DW, /EC=HIGH
09H	3002	MOVE DA PART 2 TO LANCAM
09H	5000	DW, /EC=LOW
0AH	200B	WAIT FOR MATCH, IF NO MATCH EXECUTE AT ADDRESS 0BH
0AH	F000	
0BH	0000	END
0BH	F000	

Figure 11: DA Comparison (Routine 0)

Address	Data	Comments
26H	0300	NOP
26H	2000	CW, /EC=HIGH UNLOCK DAISY CHAIN, AND/OR COMPLETE PREVIOUS INSTRUCTION
27H	0210	TCO SC
27H	2000	CW, /EC=HIGH
28H	18C0	DCS=00, DCE=11, DSC=00
28H	2000	CW, /EC=HIGH
29H	0100	SPD CR
29H	2000	CW, /EC=HIGH
2AH	0B0C	MOVE MR1, AAAH
2AH	2000	CW, /EC=HIGH
2BH	0000	CAM ADDRESS 000H
2BH	2000	CW, /EC=HIGH
2CH	8000	8000H
2CH	6000	DW, /EC=HIGH
2DH	3000	MOVE DA PART 0 TO LANCAM
2DH	7000	DW, /EC=HIGH
2EH	3001	MOVE DA PART 1 TO LANCAM
2EH	7000	DW, /EC=HIGH
2FH	3002	MOVE DA PART 2 TO LANCAM
2FH	5000	DW, /EC=LOW
30H	2031	WAIT FOR MATCH, IF NO MATCH EXECUTE AT ADDRESS 31H
30H	F000	
31H	0000	END
31H	F000	

Figure 13: DA Comparison (Routine 2)

Address	Data	Comments
0CH	0300	NOP
0CH	2000	CW, /EC=HIGH
0DH	0210	TCO SC
0DH	2000	CW, /EC=HIGH
0EH	18C0	DCS=00, DCE=11, SCS=00, SCE=11 DSC=00, SSC=00
0EH	2000	CW, /EC=HIGH
0FH	0100	SPD CR
0FH	2000	CW, /EC=HIGH
10H	0000	SPS CR
10H	2000	CW, /EC=HIGH
11H	0B0C	MOV MR1, AAAH
11H	2000	CW, /EC=HIGH
12H	0000	CAM ADDRESS 000H
12H	2000	CW, /EC=HIGH
13H	4047	MOVE DATA FROM ADDRESS 47H
13H	7000	DW, /EC=HIGH
14H	3003	MOVE SA PART 0 TO LANCAM
14H	7000	DW, /EC=HIGH
15H	3004	MOVE SA PART 1 TO LANCAM
15H	7000	DW, /EC=HIGH
16H	3005	MOVE SA PART 2 TO LANCAM
16H	5000	DW, /EC=LOW
17H	201E	WAIT FOR MATCH, IF NO MATCH EXECUTE AT ADDRESS 1EH
17H	F000	
18H	032C	MOV HM, CR, V
18H	0000	CW, /EC=LOW
19H	7000	MOVE CR SEG.0 TO FIFO
19H	D000	DR, /EC=LOW
1AH	7000	MOVE CR SEG.1 TO FIFO
1AH	D000	DR, /EC=LOW
1BH	7000	MOVE CR SEG.2 TO FIFO
1BH	D000	DR, /EC=LOW
1CH	7000	MOVE CR SEG.3 TO FIFO
1CH	D000	DR, /EC=LOW
1DH	0000	END
1DH	F000	
1EH	0000	NOP
1EH	2000	CW, /EC=HIGH
1FH	0334	MOV NF, CR, V
1FH	2000	CW, /EC=HIGH
20H	0504	CMP V
20H	0000	CW, /EC=LOW
21H	7000	MOVE CR SEG.0 TO FIFO
21H	D000	DR, /EC=LOW
22H	7000	MOVE CR SEG.1 TO FIFO
22H	D000	DR, /EC=LOW
23H	7000	MOVE CR SEG.2 TO FIFO
23H	D000	DR, /EC=LOW
24H	7000	MOVE CR SEG.3 TO FIFO
24H	D000	DR, /EC=LOW
25H	0000	END
25H	F000	

Figure 12: SA Comparison (Routine 1)

Address	Data	Comments
32H	0300	NOP
32H	2000	CW, /EC=HIGH UNLOCK DAISY CHAIN, AND/OR COMPLETE PREVIOUS INSTRUCTION
33H	0210	TCO SC
33H	2000	CW, /EC=HIGH
34H	18C0	DCS=00, DCE=11, DSC=00
34H	2000	CW, /EC=HIGH
35H	1000	SPD CR
35H	2000	CW, /EC=HIGH
36H	0B0C	MOV MR1, AAAH
36H	2000	CW, /EC=HIGH
37H	0000	CAM ADDRESS 000H
37H	2000	CW, /EC=HIGH
38H	0000	0000H
38H	6000	DW, /EC=HIGH
39H	4048	MOVE DATA FROM ADDRESS 48H
39H	7000	DW, /EC=HIGH
3AH	4049	MOVE DATA FROM ADDRESS 49H
3AH	7000	DW, /EC=HIGH
3BH	404A	MOVE DATA FROM ADDRESS 4AH
3BH	5000	DW, /EC=LOW
3CH	042D	VBC HM,E
3CH	0000	CW, /EC=LOW
3DH	0000	END
3DH	F000	

Figure 14: Purge on Address (Routine 3)

Address	Data	Comment
3EH	0300	NOP
3EH	2000	CW, /EC=HIGH UNLOCK DAISY CHAIN, AND/OR COMPLETE PREVIOUS INSTRUCTION
3FH	0210	TCO SC
3FH	2000	CW, /EC=HIGH
40H	0004	DCS=00, DCE=00, DSC=00
40H	2000	CW, /EC=HIGH
41H	1000	SPD CR
41H	2000	CW, /EC=HIGH
42H	0B0C	MOV MR1, AAAH
42H	2000	CW, /EC=HIGH
43H	0001	CAM ADDRESS 001H
43H	2000	CW, /EC=HIGH
44H	404B	MOVE DATA FROM ADDRESS 4BH
44H	5000	DW, /EC=LOW
45H	043D	VBC ALM, E
45H	2000	CW, /EC=HIGH
46H	0000	END
46H	F000	

Figure 15: Purge on Associated Data (Routine 4)

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