MU9C8338A/MU9C8338 Differences

INTRODUCTION

The MUSIC Semiconductors MU9C8338A Ethernet Filter Interface is a single port 10/100Mbps Ethernet filter device capable of performing all the necessary address processing functions in a typical bridging or switching application. This device is an enhanced version of the original MU9C8338 Ethernet Filter, with additional functionality for multicast address processing.

The MU9C8338A is backward compatible with the MU9C8338 and fits exactly into existing designs employing the MU9C8338.

This note explains differences between the MU9C8338A and the MU9C8338.

PINOUT

The MU9C8338A is pin compatible with the MU9C8338. No pins are added, removed, or changed. Both devices use the same 144-pin LQFP package.

NEW CHIPROL OPERATION

The MU9C8338 Single Port device inherits its features from the original MUSIC Semiconductors MU9C8358 Quad Ethernet Filter Interface. Two quad devices can be connected, providing support for eight 10/100Mbps ports. This requires a register specifying one device as the master and one as the slave. This register is the CHIPROL register and is designated as 1H for Slave and 0H for Master. The default setting for this register is Slave mode, therefore during initialization, one device is configured to be the Master prior to other operations.

When the MU9C8338 was initially designed, this register function was left intact although a single device was the only recommended application. Therefore, the register defaulted to 1H (old Slave mode) and must be set to 0H prior to any other initialization.

The MU9C8338A has a minor change causing this register to default to 0H (old Master mode). Consequently, the device resets to a mode allowing access to all the registers. It is unnecessary to set this register prior to system register access, as was the case with the MU9C8338. Although the CHIPROL register is still shown in the MU9C8338A data sheet, it is redundant because no initialization is required. The register remains to allow backward compatibility.

The change in the register default setting should not affect existing MU9C8338 designs using the MU9C8338A as a replacement. This is because existing CHIPROL register access by system software overwrites the register with the same value. The register access is redundant but can remain in the existing initialization because it does not cause the device to malfunction.

REGISTER ACCESS

The MU9C8338 contains registers that can be written to but not read from, making it impossible to verify the contents of the registers during initialization. This annoying feature was removed from the MU9C8338A, making it possible to read these registers as well as write to them. The registers that have been made R/W are shown in Table 1. This change should not affect existing designs using the MU9C8338A to replace a MU9C8338, because any register access software operates as originally designed.

Table 1: Registers with R/W Access in MU9C8338A but not in MU9C8338

Register	Address	MU9C8338	MU9C8338A
SSCFG	SYSTEM_BASE+1H	W	R/W
SDCFG	SYSTEM_BASE+2H	W	R/W
STARG	SYSTEM_BASE+3H	W	R/W
SMXSADACYC	SYSTEM_BASE+CH	W	R/W
SSAU	SYSTEM_BASE+10H	W	R/W
SSAL	SYSTEM_BASE+11H	W	R/W
CHIPROL	CHIP_BASE+1H	W	R/W
PID	CHIP_BASE+40H	W	R/W
PCFG	CHIP_BASE+41H	W	R/W
PTARG	CHIP_BASE+42H	W	R/W

NEW REGISTER

A new register is added to the MU9C8338A. This register is named the Port Configure Extended register (PCFG_EXT) and allows the new MU9C8338A features to be enabled. The register is accessed using the /PCS signal and is located at address 44H (offset from the chip base address). This register defaults to the value 0H, which disables all of the additional features. This allows the MU9C8338A to be backward compatible with existing designs using the MU9C8338. Existing MU9C8338 designs operate normally when the register is left with its default setting.

NEW MULTICAST PROCESSING FEATURES

The MU9C8338A offers additional functionality that allows frames with multicast group addresses to be processed. System software is required to add the known group addresses to the LANCAM database using the built-in add entry routine. Subsequently, after the entries are added, the MU9C8338A is able to process multicast frames in the same way as it processes unicast frames.

This is a desirable new feature because the MU9C8338 processes only unicast frames. Previously, all multicast frames were forwarded even when there was no need to do so. The new multicast processing feature allows the MU9C8338A to process multicast frames automatically, therefore reducing the transmission of unwanted multicast traffic across the switching or bridging system.

Setting bits 1 and 2 in the PCFG_EXT register enables the new features. Setting bit 1 to one enables multicast destination address processing. Additionally, setting bit 2 to one allows the MU9C8338A to process the source addresses of multicast frames. When the multicast DA processing is enabled, the system can specify the default action for instances when a matching address is not found in the LANCAM database. Bit 0 of the register is used to specify how the frame is treated when this occurs. If it is set to zero, the REJ output is asserted, causing the multicast frame to be rejected. Conversely, setting the bit to one causes the frame to be forwarded because REJ is not asserted.

Any existing MU9C8338 designs operate normally with a MU9C8338A as a replacement, if the register is left with its default setting. This disables the multicast processing features and causes the MU9C8338A to operate identically to the MU9C8338.

NEW PERMANENT ENTRY FUNCTIONALITY

The MU9C8338A offers additional functionality allowing permanent entries to be handled differently than the way they were handled by the MU9C8338. When the SA processing function is enabled in the PTARG register, the MU9C8338 either learns new SAs or updates existing addresses, if they are found in the LANCAM database. When the entry is found to be in the LANCAM, the SA, timestamp, and port ID are overwritten through a mask register. During system initialization, typical applications have the mask register loaded with a value ensuring that the permanent bit is not changed. Therefore, permanent entries, added by the system software, are not inadvertently made non-permanent.

Although this method of updating entries ensures permanent entries remain in the database, it also allows them to have their port ID changed. In most applications, this is permissible, because the database automatically tracks where Ethernet addresses are located within the network regardless of whether they are permanent. Unfortunately, it is sometimes a drawback to have the port ID of a permanent entry changed automatically by the SA learn routine.

To overcome the problem of permanent entry modification, an additional feature is added to the MU9C8338A. This allows the SA learn built-in routine to read the associated data from the LANCAM upon finding a matching entry. When this is done, the routine checks bit 15 to determine if the entry has been marked as a permanent entry. If it has, the entry is left untouched, thus allowing the port ID to remain the same. If the entry is found to be a normal non-permanent entry, it is updated in the normal way.

This new feature is enabled by setting bit 3 to one in the PCFG_EXT register. Existing MU9C8338 designs operate normally with a MU9C8338A replacement, if the register is left with its default setting. This default setting causes the SA built-in routine to operate identically to the routine in the MU9C8338.

FULL FLAG INTERRUPT

The MU9C8338 has a bug, which is described in the associated Errata, that affects the way the full flag interrupt is triggered. As explained in the data sheet, when the interrupt is enabled, it is triggered when the MU9C8338 /FI input is asserted LOW. This is the normal result when the attached LANCAM database becomes full, because the LANCAM /FF changes from logic 1 to logic 0.

Unfortunately, the MU9C8338 has a bug that causes the Interrupt condition to operate opposite from what is expected. Instead of a HIGH to LOW transition causing the interrupt, a LOW to HIGH transition causes it. This is explained in Problem 1 of the *MU9C8338/8358L Ethernet Filter Interface Errata Sheet*. The Errata also explains that the problem can be fixed by placing an inverter between the LANCAM /FF output and the MU9C8338 /FI input. It is recommended that the inverter circuit be designed to be bypassed, if necessary. This allows new revisions of the properly operating MU9C8338, to be used on the same circuit board, with the inverter bypassed.

The bug is now fixed, therefore, the MU9C8338A does not suffer from the full flag interrupt problem. The MU9C8338A now operates as originally expected. When the MU9C8338A is used in an existing MU9C8338 application, special care must be taken if the existing system uses the interrupt. When an inverter was used to overcome the problem, it should be bypassed, allowing the new MU9C8338A application to operate properly.

Some existing applications may monitor the status of the SSTAT register to determine if the LANCAM database is full. In designs using this method instead of the interrupt, bit 0 of SSTAT indicates the state of the LANCAM in the same way as before. Therefore, when bit 0 is one, the LANCAM is not full, and when bit 0 is zero, the LANCAM is full.

The MU9C8338/8358L Errata Sheet also documented a problem with the method for resetting the interrupt once an interrupt has occurred. This problem exists in the MU9C8338 and MU9C8338A. Therefore, existing MU9C8338 applications that follow the method shown in the Errata Sheet will operate normally when using the MU9C8338A as a replacement.

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