Using the MU9C8338A Ethernet Filter with Motorola PowerQUICC Processors

INTRODUCTION

The MUSIC MU9C8338A is a single-port 10/100Mb Ethernet filter interface, ideal for filtering or bridging applications. It is a single-port version of the MU9C8358L quad-port 10/100Mb Ethernet Filter Interface. The MU9C8338A features a high-performance, large capacity Ethernet address processing subsystem when used with the MUSIC LANCAM B Family. The MU9C8338A accelerates single-port Ethernet address filtering functions as seen in Wireless LAN (WLAN) applications.

The MPC860 PowerQUICC series is widely used in communications and networking applications, and is offered in a wide variety of configurations. The MUSIC MU9C8338A can be paired with the MPC860T or equivalent, extending both its capability and application. Some of these processors, such as the MPC860T, incorporate a 10/100Mb Ethernet controller.

This Note focuses on interfacing the MUSIC MU9C8338A with the popular Motorola MPC860 PowerQUICC processors.

MU9C8338A Description

The MU9C8338A 10/100Mb Ethernet address filter is a hardware parse engine and Content Addressable Memory (CAM) controller. It acquires the inbound Ethernet frame from the Physical Layer device (PHY) on the receive side of the Media Independent Interface (MII) bus, and extracts the Destination address (DA) and Source address (SA) from the frame.

Upon receipt of the DA, the MU9C8338A compares the DA to the address database maintained in the attached LANCAM(s). When certain criteria are met, the MU9C8338A asserts a REJECT signal, indicating that the frame is not to be copied, processed, or forwarded.

Upon receipt of the SA, the MU9C8338A compares the SA to the address database. Upon a match, the timestamp and incoming port ID are updated. When no match occurs, the address is learned, along with the current timestamp and incoming port ID. Automatic Learning may be turned off.

The MU9C8338A also offers the option to process multicast addresses in addition to unicast. This allows applications, such as Wireless Access Points, to reduce the transmission of unnecessary multicast traffic. Multicast group addresses can be added to the address database by system software. The MU9C8338A can be configured to forward or reject Multicast packets not matching the known addresses. This allows the system designer maximum flexibility when deciding how the application should deal with multicast.

If an Ethernet address in the database is inactive for a pre-determined period of time, the MU9C8338A automatically ages out that address, removing it from the LANCAM database. Automatic aging is activated either by the CPU accessing a MU9C8338A internal register or by hardware asserting an input pin.

All of the above operations can occur without host processor intervention. The host processor is responsible for adding, maintaining, and deleting static (permanent) addresses in the LANCAM database. These LANCAM routines are built into the MU9C8338A, but are initiated by the host processor. In addition, the host processor has access to other supervisory routines built into the MU9C8338A, and can control the LANCAM through the processor interface of the MU9C8338A.

Interface Overview

The interface between the MU9C8338A and MPC860, shown in Figure 1, requires a minimal amount of logic and configuration. The two interface sections in this note address connectivity to the MII bus and the MU9C8338A host CPU interface. An additional section discusses cascading LANCAMs to provide a deeper address database.

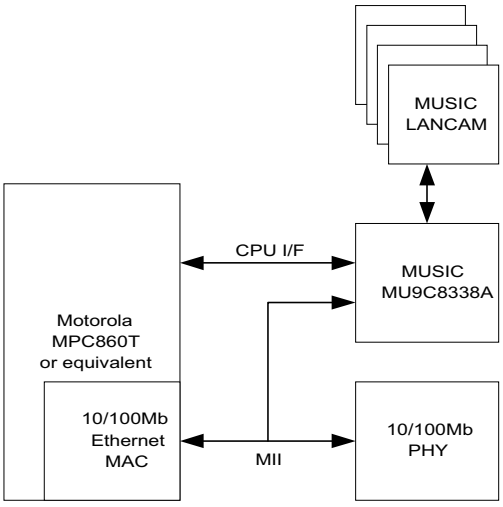

Figure 1: MU9C8338A with MPC860T

MII HARDWARE INTERFACE

The MU9C8338A originally was designed for use with discrete PHYs and Media Access Controllers (MACs). Most discrete MACs have an input reject signal that is asserted to reject the frame that is currently being received. This allows the MU9C8338A output REJ signal to be connected directly to the MAC. When the MU9C8338A determines that the frame should be rejected, then the signal is asserted, discarding the frame.

The internal MPC860T Ethernet MAC interface incorporates the IEEE standard MII connections. The MPC860T does not have a reject input signal similar to the ones found in discrete MACs. Therefore, when using the MPC860T, a rejection mechanism must be created utilizing the existing MII signals.

MII Rejection Mechanism

The MU9C8338A snoops the receive side of the MII to gather the Ethernet DA and SA of an incoming frame. It asserts the REJ output signal to force the rejection of a frame.

There are two signals within the MII that cause the MPC860T MAC to reject a frame. These are RX_DV (Receive Data Valid) and RX_ER (Receive Error). Both of these signals along with RX_DATA are synchronous with RX_CLK (Receive Clock).

RX_ER is asserted for at least one clock cycle when an error is detected by the PHY during frame reception. Therefore, in a typical application not containing a MU9C8338A, the PHY RX_ER output is connected directly to the MAC RX_ER input. This ensures that frames with errors detected by the PHY can be rejected before being fully received.

RX_DV is asserted while valid data is present on the RX_DATA bus. If a MAC detects that the RX_DV signal was not HIGH for at least 64 bytes of receive data, it determines that the packet has a minimum packet length error. A minimum packet length error is caused because the Ethernet packet size was less than 64 bytes. This error is also known as a runt packet error. The PHY also uses the RX_DATA and RX_DV signals in conjunction with the RX_ER signal to indicate coding errors.

Therefore, the MU9C8338A could reject frames by asserting the MPC860T RX_ER input or by prematurely forcing the RX_DV input LOW. Unfortunately, most network management software treat frame errors seriously. If the MAC RX_ER input is used by the MU9C8338A to force frames to be rejected, then a false number of frame errors are reported.

In contrast, runt packet errors are treated less seriously by network management software and are much easier to deal with. Therefore, this note explains in detail how to implement the reject mechanism by forcing RX_DV inactive during frame reception. The PHY and MAC RX_ER signals are not discussed further with respect to rejecting frames.

The MU9C8338A parses the Ethernet DA and SA from the inbound frame and performs the necessary LANCAM database operations. When it is determined that a frame is not to be forwarded, the MU9C8338A asserts the REJ signal soon after the addresses are received. During the reception of the frame, RX_DV is asserted HIGH by the PHY, indicating that the data on the RX_DATA bus is valid. When the REJ signal causes the RX_DV signal, which is currently HIGH, to be forced LOW for the remainder of the frame, the frame is rejected as a runt packet.

The number of runt packets received is kept as a statistic within the MPC860T MAC. If it is important to keep statistics of runt frames, the REJ output of the MU9C8338A can be used to increment a counter. The value of this counter subtracted from the runt packet counter yields a true runt frame statistic.

Two proposed implementations of the MII rejection circuitry are given, allowing the designer to choose which one best fits the design. The first solution uses low propagation delay discrete logic. The second solution allows for the use of slower logic devices, such as the logic in programmable devices.

In both cases, the RX_DV from the PHY is gated by a latched version of the MU9C8338A REJ signal. Upon assertion of the REJ signal, RX_DV is forced LOW for the remainder of the frame. The critical timings to be met are the MPC860T MAC setup and hold times with respect to RX_CLK.

MII REJECT using Discrete Logic

The discrete logic solution is given because of its low propagation times and simplicity. The following bullets offer a detailed analysis that assumes the selected PHY vendor meets the 10 nS setup time stated in the IEEE specifications.

The analysis shows some specific timing specifications that the user should keep in mind when employing the discrete logic solution. Also note that the REJ signal used in this solution is programmed to be active low and, consequently, is referred to as /REJ. Please refer to Figure 2 for connection details.

- Use the SN74ALVC08 to gate RX_DV with the latched MU9C8338A /REJ signal.

  This gate has a maximum propagation delay of 3 nS, and meets MPC860's RX_DV setup time. The MPC860 RX_DV input setup and hold times of 5 nS must be met.
- The /REJ signal changes state 10 nS minimum to 20 nS maximum after rising edge of RX_CLK.
- Tpd from CLR input to Q output is 1 nS minimum to 5.4 nS maximum for the SN74LVC74A flip-flop.
- Tpd from REJ to 860_DV is 11 nS minimum to 25.4 maximum from rising edge of RX_CLK.
- 11 nS meets 860_DV hold time and 14.6 nS (40 - 25.4) meets 860_DV setup time for next clock edge.

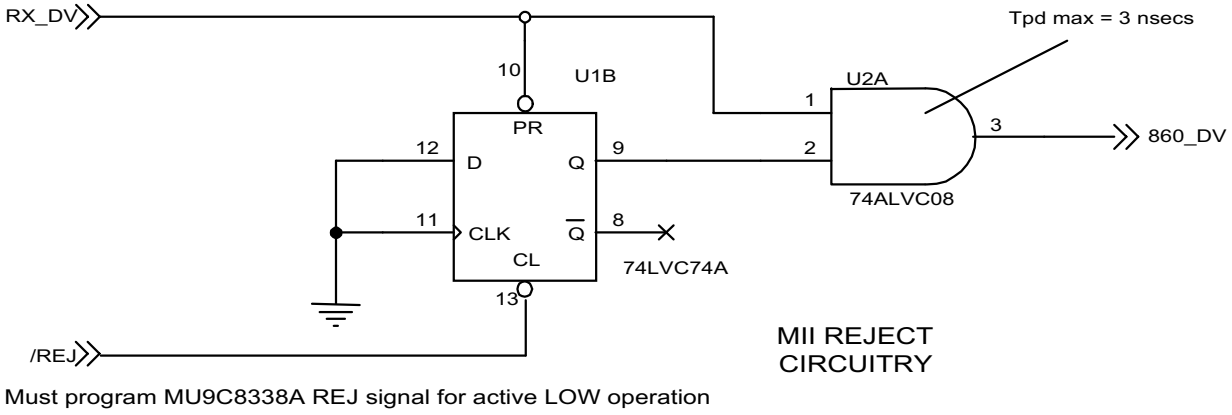

Figure 2: MU9C8338A Packet Rejection Circuit - Discrete Logic

MII REJECT using Programmable Logic

The second solution, shown in Figure 3, utilizes the same logic as discrete circuitry (shown in Figure 2) but the timings for the MII rejection circuitry can be relaxed. Key to this solution is maintaining alignment of RX_DV, RX_ER, and RX_DATA with respect to RX_CLK. Therefore, if RX_DV is delayed one 25 MHz clock cycle by the MII rejection circuitry, RX_ER and RX_DATA also are delayed by the same amount of time.

The design must still meet the MPC860T 5 nS setup and hold times with respect to the RX_CLK. Misalignment of data with respect to RX_DV causes Frame Check Sequence (FCS) errors and is interpreted by the MAC as frames with errors. Similarly, misalignment of RX_ER with RX_DATA causes other serious problems. With this in mind, due care must be taken to meet the 5 nS setup and hold times discussed earlier.

The Reject Mechanism block shown in Figure 3 is the packet rejection circuit shown in Figure 2. The D-type flip-flops, also shown in Figure 3, maintain the alignment of RX_DV, RX_ER, and RX_DATA.

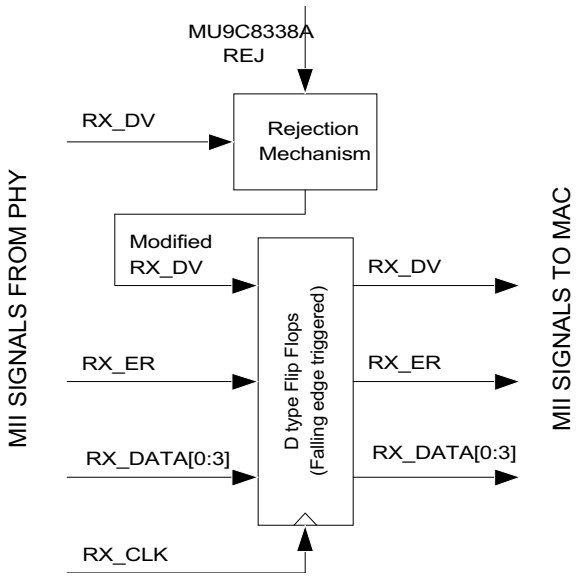

Figure 3: Rejection Circuit - Programmable Logic

Runt Statistics Counter Implementation

As discussed earlier, a rejection counter is needed when the runt packet statistics are needed. A counter is increased by one every time the MU9C8338A asserts the REJ signal. This REJ counter is subsequently read every time software determines the number of runt packets. In order to calculate the true number of runt packets, software subtracts the REJ counter from the MAC runt statistics counter.

One of the four MPC860 general-purpose timers can maintain the REJ assertion count. The following gives some general information about using the internal MPC860 counters.

Connect the MU9C8338A /REJ signal to the TINx (x indicates timer 1 through 4) MPC860 timer input that is chosen for the REJ counter. The timer should be configured to increment on a falling edge clock on the TINx MPC860 input.

The counter is 16 bits wide and can be cascaded with another counter to be 32 bits wide. The counter also can be configured to generate an interrupt at a programmed value, such as at the roll-over condition. The roll-over condition is when a counter indicating 0xFFFF is increased by one, rolling over to 0x0000.

The counter should be cleared prior to initialization of the MUC98338A and LANCAM(s). This ensures that the counter maintains a proper count and doesn't miss reject pulses. If the counter is cleared after the initialization of the MU9C8338A and LANCAM has occurred, one or more reject pulses may be cleared inadvertently and therefore not counted.

The TINx input timing specification requires that the input remain LOW for at least one MPC860 clock cycle and HIGH for at least two clock cycles, which is 20 nS and 40 nS respectively at 50 MHz. The minimum LOW time for /REJ is 110 nS and worst case minimum HIGH time is several 25 MHz clock cycles between /REJ pulses, which satisfies the TINx specification.

PROCESSOR INTERFACE

The MU9C8338A processor interface is a word-wide asynchronous interface and addressed as Little Endian (least significant byte/word stored at lowest address). The MPC860 external bus is synchronous and defaults to Big Endian mode of operation. The MPC860 also operates in two other bus modes: Little Endian and Munged Little Endian, which is a Power PC specific version of Little Endian.

The following section covers synchronizing the MPC860 external bus with the MU9C8338A processor interface and connecting the MPC860 address and data bus in different Endian modes.

Processor Bus Synchronization

The MPC860 external interface is synchronous with the MPC860 CLKOUT signal. To run the 10/100Mb Ethernet interface without buffer under-runs and over-runs using external SDRAM, the MPC860 must be run at 50 MHz or higher. The MU9C8338A processor interface is an asynchronous interface, which uses its PROC_RDY output to control the flow of data to and from the device internal registers.

When data is being written to an internal register, the PROC_RDY signal is asserted when the data has been latched. Conversely, when data is being read from an internal register, the PROC_RDY signal is asserted when the MU9C8338A has placed valid data on the data bus.

The MPC860 external bus control signals are programmable and can be configured to meet the MU9C8338A timing specifications. The exception to this is the MPC860 ready input signal, which is the Transfer Acknowledge (/TA) input required to be synchronous with CLKOUT. Therefore, the PROC_RDY signal must be synchronized externally, inverted, and meet the required setup and hold times for the MPC860 /TA input. This is done by using a D-type edge triggered flip-flop. Alternatively, the MPC860 User Programmable Machine may be employed when a glueless interface is required. Both methods are explained in the following sections.

Processor Bus Synchronization Using External Circuitry

The discreet device MII reject circuitry, shown in Figure 2, is implemented using one of two flip-flops from a 74LVC74A dual D-type edge-triggered flip-flop IC. The circuit shown in Figure 4 on page 5, utilizes the remaining D-type flip-flop from the same 74LVC74A device to implement the processor-ready circuit. The timings for the simple synchronization circuit with the MPC860 running at 50 MHz are:

- The MPC860 /TA setup time is 9.75 nS, with a hold time of 1nS.
- The MU9C8338A generates PROC_RDY 8nS after the rising edge of MU9C8338A clock input, and must be inverted.
- Use an external flip-flop, which is clocked by the MPC860 CLKOUT, and connect /TA to the /Q output.

This method allows the MU9C8338A to be operated by a clock other than the processor clock.

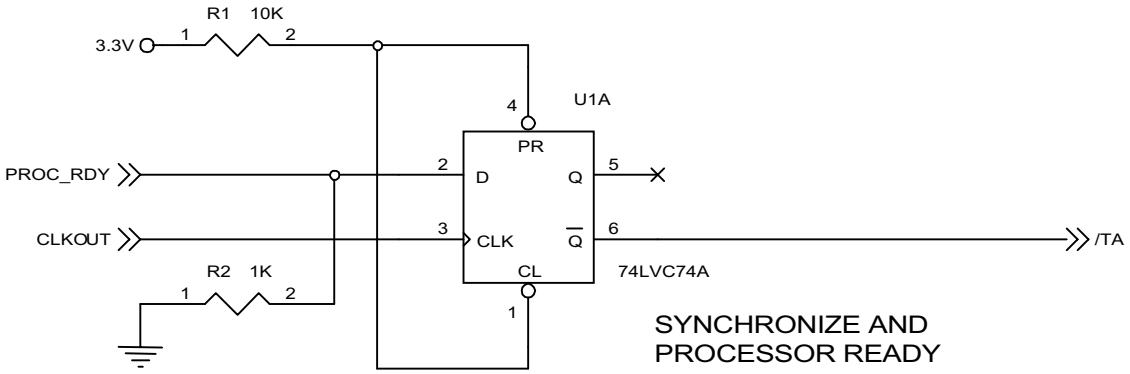

Figure 4: MU9C8338A Processor Ready Circuit

Processor Bus Synchronization with User Programmable Machine

An alternative method, which avoids external glue logic, is to employ the MPC860 User Programmable Machine (UPM), which provides the proper interface timing to the MU9C8338A. The UPM has an asynchronous ready input and can use the asynchronous PROC_RDY signal because it is supplied by the MU9C8338A.

The UPM is a state machine driven by user programmable RAM. The designer must generate the correct RAM entries required for each read and write access. This process requires additional effort from the designer but provides a glueless processor interface.

Data and Address Buses

The MU9C8338A processor interface consists of a 16-bit data bus, 8-bit address bus and necessary control signals. Each 16-bit wide internal register is addressed on a word-by-word basis.

The MU9C8338A data sheet identifies the data bus as D[15:0] and the address bus as A[7:0]. Consequently, the least-significant bit of both buses is bit 0. Therefore, the most-significant bit of the data bus is bit 15 and the address bus is bit 7.

The Motorola MPC860 processors, which are discussed throughout this note, use an alternative bus naming convention. The data bus is always shown as D[0:31]. Similarly, the address bus is shown as A[0:31]. Therefore, the least-significant bit is bit 31 and the most significant is bit 0.

The processor's bus operation default mode is Big Endian. This is the most popular mode of operation and is very common in most MPC860-based designs. When using the MPC860 in this mode, the user can connect the address and data buses directly to the MU9C8338A. This is the recommended mode of operation because the design goal is to minimize any byte or word swapping in software when accessing the MU9C8338A host CPU registers.

The MPC860 has two other modes of operation: true Little Endian and Munged Little Endian, which is a Power PC specific version of Little Endian. These different MPC860 modes have implications for both connectivity and register accesses. The next sections explain each mode in detail.

Big Endian

Figure 5 shows the necessary address and data bus connections for Big Endian mode. The data bus can be connected directly between the processor and the MU9C8338A. The MPC860s lowest order address bit is not used because the MU9C8338A internal registers are word addressable and not byte addressable.

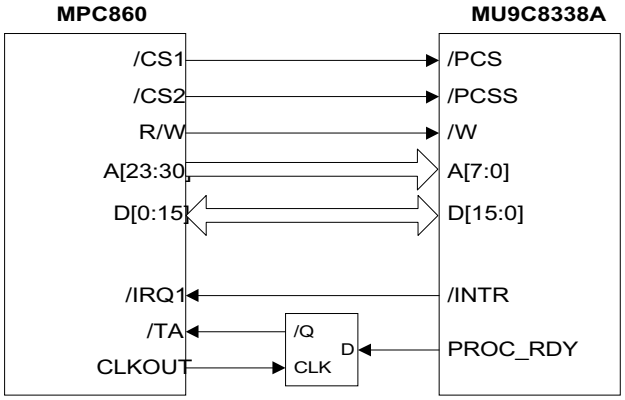

Figure 5: Connections for Big Endian and Munged Little Endian Modes

True Little Endian

Figure 6 shows the necessary address and data bus connections for True Little Endian mode. When using the MPC860 in this mode, it is beneficial to perform the byte swapping operation in hardware instead of software. Therefore, bits 0 - 7 and 8 - 15 of the data bus are swapped. The MPC860's lowest order address bit is not used because the MU9C8338A internal registers are word addressable and not byte addressable.

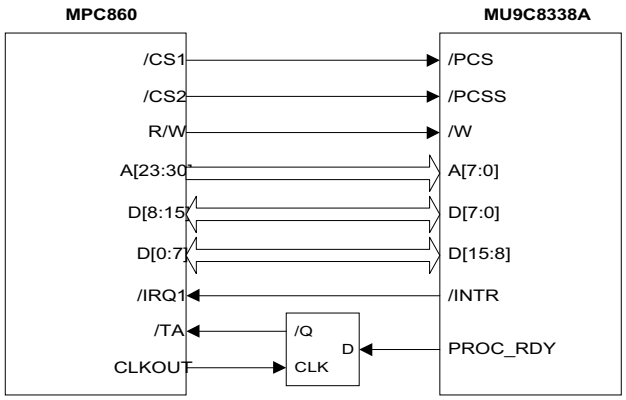

Figure 6: True Little Endian Mode Connections

Power PC Specific (Munged) Little Endian

Figure 5 on page 5 shows the necessary address and data bus connections for the Power PC specific Little Endian mode. This mode is sometimes referred to as Munged Little Endian because of the way the address is altered. This mode uses the same byte-ordering scheme as Big Endian but it modifies, or munges, the address.

The modification involves the three low order bits of the MPC860 address output being exclusive-ORed with the binary value 110. For 16-bit accesses this modification only affects A30 and A29 because the word-wide accesses does not require A31 to be used. Table 1 shows how the address bus differs between modes when accessing the first six MU9C8338A System registers.

When Big or Little Endian mode is used, it can be seen that the MPC860 address bus operates normally when attempting to address any of the MU9C8338A registers. In both modes, A[23:30] corresponds directly to the address of the register that is being accessed.

However, in Munged Little Endian Mode, the address bits are modified as described earlier. This means that A30 and A29 are exclusive-ORed with the binary value 11. Therefore, when addressing the STARG register at MU9C8338A address 03H, the MPC860 outputs 00H on A[23:30]. In Munged Little Endian mode, the software memory mapping used for each of the MU9C8338A registers must be tailored to suit the new munged address values.

Table 1: Munged and Non-Munged Address Bus Differences

MU9C8338A Register Name	MU9C8338A A[7:0]	MPC860 A[23:30]	
		Munged Little Endian	Big or Little Endian
SSTAT	00H	03H	00H
SSCFG	01H	02H	01H
SDCFG	02H	01H	02H
STARG	03H	00H	03H
SCDW0	05H	06H	05H
SCDW1	06H	05H	06H

MU9C8338A Processor Port Control Signals

The MU9C8338A has two chip select signals: /PCS and /PCSS. The /PCS input grants access to the port and chip registers of the MU9C8338A. The /PCSS input grants access to the system registers of the MU9C8338A. The appropriate signal should be asserted by the MPC860 to access the correct register. The MU9C8338A responds by asserting its PROC_RDY output to complete the processor cycle.

The /W input of the MU9C8338A controls the direction of data flow to and from the Ethernet filter chip. The signal should be HIGH when writing to a register and LOW when reading a register.

The /INTR output of the Ethernet filter chip is programmable, selecting which events generate an interrupt. When you want the processor to read the results of an Ethernet address search through the processor port, program the MU9C8338A to generate an interrupt for each DA search. An interrupt also may be generated when the attached LANCAM database becomes full.

In most applications, system hardware determines if a packet is accepted or rejected. Therefore, it is unnecessary for the processor to read the resulting information after every DA search, and the /INTR signal does not have to be used or connected.

LANCAM DATABASE

The MU9C8338A Ethernet Filter is designed to work seamlessly with MUSIC's LANCAM B devices. The filter automatically performs the operations required to store the Ethernet database in the attached LANCAM(s). The LANCAM database consists of the Ethernet addresses along with their port ID, time-stamp, and permanent entry indicator.

The MU9C8338A has a glueless interface that allows the user to connect a LANCAM B without the need for extra logic. Although the interface allows the use of devices that have as many as 8192 memory locations, a larger database is sometimes required, in which case, LANCAMs may be cascaded, providing a much larger database.

Cascading LANCAMs

MUSIC LANCAMs can be cascaded to any practical depth. The LANCAM control state machine within the MU9C8338A allows up to four devices to be connected without the need for external logic. Figure 7 shows how four devices are cascaded.

Each of the four devices has match flag signals connected in such a way that a match passes or ripples through all the devices in the chain. The full flag signals are connected in a similar way, which determines when the integrated system becomes full. This system is known as "daisy-chaining" because match and full flags are connected to form a chain.

The connections, when cascading devices in this way, are very straightforward. Each of the four devices shown shares a common data bus (DQ [15:0]). They also share a common control bus, which consists of the /EC, /CM, /W and /E signals. Both of these buses are connected directly to the corresponding MU9C8338A signals.

The /FI input of LANCAM 0 is connected to GND and the /MI input is connected to VDD. When using LANCAM B family devices, the /MI input is connected 3.3v. It is recommended (although not shown in Figure 7) that pull-up/pull-down resistors be used.

The /FF and /MF outputs of LANCAM 0 are connected to the /FI and /MI inputs of LANCAM 1. This is repeated for each of the four LANCAMs shown. Finally, the /FF output of LANCAM 3 is connected to the MU9C8338A /FI input and the /MF output is connected to the /MI input. When two or three devices are cascaded, the /FF and /MF outputs of the last device are connected to the MU9C8338A.

Although Figure 7 shows four cascaded devices, the cascade logic supports an arbitrary number of devices. However, PCB real estate, signal integrity, and capacitance place limits on practical cascade depth.

Another limiting factor is flag-ripple timing delays. These are caused when the state of each device in the chain must report the state of the match and full flags to the next device. The MU9C8338A allows the connection of up to four devices. When a user must build a database requiring more than four LANCAMs, an alternative cascading method must be employed. This alternative method uses external prioritization, which greatly reduces the ripple delay and allows for the use of more devices.

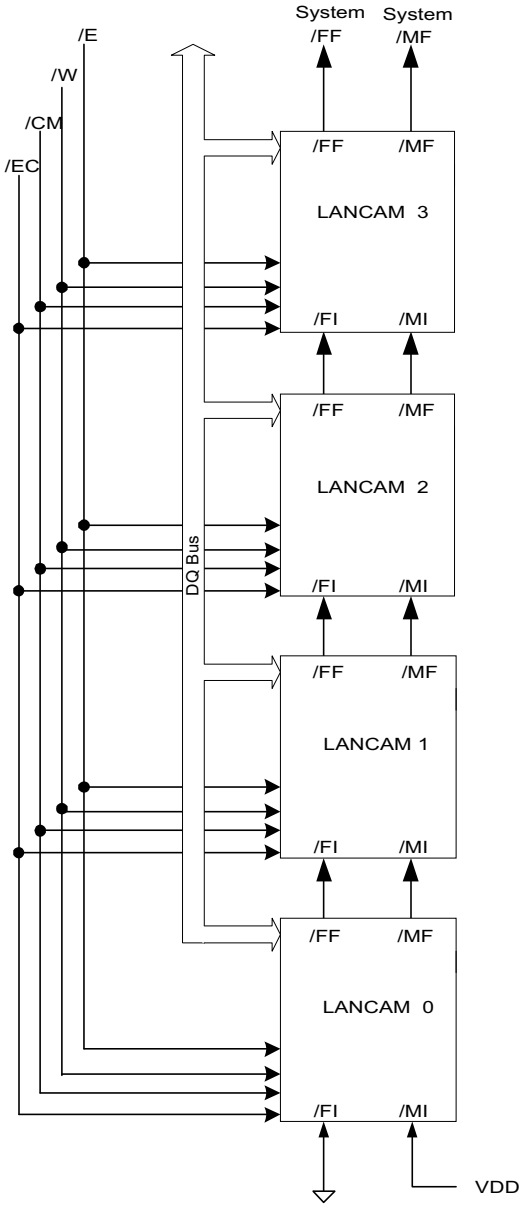

Figure 7: Cascading up to Four LANCAM Devices Using a Daisy Chain

Cascading LANCAMs with External Prioritization

The MU9C8338A LANCAM control state machine limits the system designer to four LANCAMs when the built-in cascade logic is used. In most applications, a chain of four devices is sufficient to satisfy system database requirements.

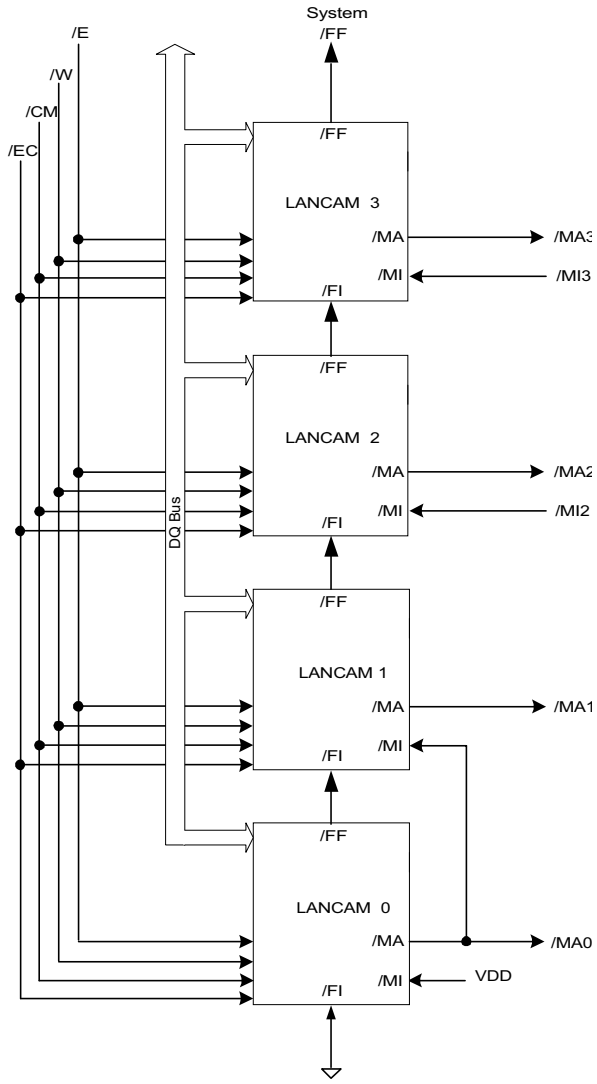

Figure 8: Cascading LANCAM Devices with External Prioritization

When more than four devices are required, the built-in cascade logic is inadequate. This is because the MU9C8338A state machine samples the match flag (/MI) input before the LANCAM chain produces a valid system match flag.

This problem is overcome with the aid of an external prioritization scheme. Figure 8 shows a chain of four devices. The /MA outputs of each LANCAM are connected to a Programmable Logic Device (PLD) that has four inputs and three outputs. The three PLD outputs are connected to the /MI inputs of LANCAM 2 and 3 and the MU9C8338A /MI input. Table 2 shows the PLD inputs, outputs, and equations. The chain is easily expanded to include additional devices by adding an input and output to the PLD.

Table 2: PLD Equations

PLD Output	Equation
/MI2	/MA0 & /MA1
/MI3	/MA0 & /MA1 & /MA2
System /MF	/MA0 & /MA1 & /MA2 & /MA3

For example, when a fifth LANCAM is added to the chain shown in Figure 8, the following is required:

- Additional PLD input = /MA4
- Additional PLD output = /MI4
- LANCAM 4 /MA connected to PLD /MA4
- LANCAM 4 /MI connected to PLD /MI4
- LANCAM 3 /FF connected to LANCAM 4 /FI
- LANCAM 4 /FF is now System /FF
- /MI4 = /MA0 & /MA1 & /MA2 & /MA3
- System /MF = /MA0 & /MA1 & /MA2 & /MA3 & /MA4

The advantage of this encoding scheme is that each LANCAM does not have wait on the previous /MF output becoming valid. Instead, there is only a single gate delay between all /MA outputs becoming valid and the MU9C8338A /MI input. The removal of this flag ripple through delay greatly increases the number of cascaded devices supported. Note that PCB real estate, signal integrity, and capacitance still are limiting factors in memory depth of the LANCAM database.

Maximum PLD Propagation Delay

During a DA processing function, the MU9C8338A samples the /MI input, determining if a match is found in the LANCAM database. The propagation delay of the external prioritization PLD must be appropriate for the speed-grade of LANCAMs being used. The delay must be small enough to allow the PLD System /MF to satisfy the MU9C8338A /MI setup time.

Figure 9 shows the relationship between the LANCAM /MA output and the MU9C8338A /MI input. The timing given in Figure 9 is explained as follows:

A 50 MHz SYSCLK is shown but any speed between 25 MHz and 50 MHz is acceptable. The MU9C8338A samples the /MI input on the third rising edge of SYSCLK after the /E output was asserted HIGH. The MU9C8338A data sheet specifies a minimum 5 ns setup time (tMIVKH) to ensure that the system match flag is latched correctly.

The MU9C8338A data sheet also states that the maximum delay from SYSCLK being asserted to /E going HIGH is 19 ns (tKHEH). Therefore, a system of cascaded LANCAMs must provide a valid match flag at the /MI input within 36 ns of /E being asserted HIGH.

As an example, when the slowest speed-grade version of LANCAM available (90 ns) is used, /MA is valid 25 ns after the rising edge of /E. This allows, in the worst case, an 11 ns delay before the /MI input is sampled. Therefore, a PLD must be chosen that has a propagation delay of 11 ns or less. Fortunately, low-cost PLDs, with propagation delays between 10 ns and 20 ns, are readily available.

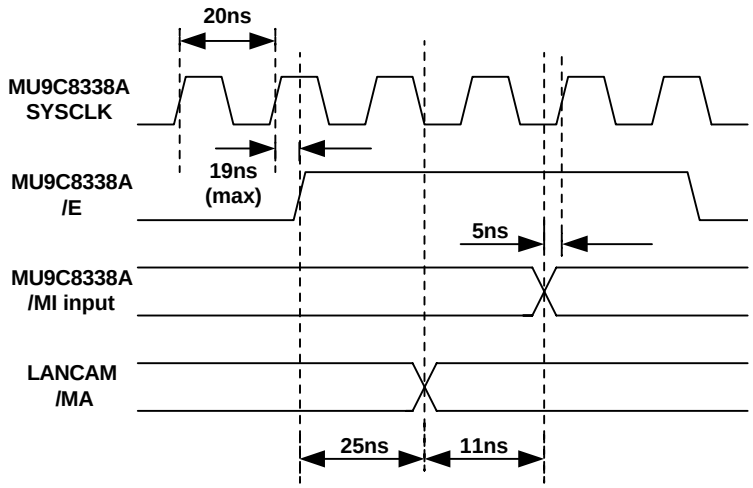

Figure 9: LANCAM /MA and MU9C8338A-90 /MI Timing Relationship

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