MU9C8338 Single-Port 10/100 Mb Ethernet Filter Users Guide

INTRODUCTION

The MUSIC MU9C8338 is a single-port 10/100Mb Ethernet filter interface ideal for filtering or bridging applications. It is a single-port version of the MU9C8358L quad-port 10/100 Ethernet Filter Interface. The MU9C8338 provides the user with a high performance, large capacity Ethernet address processing subsystem when used in conjunction with the MUSIC LANCAM B or LIST XL Families.

In a typical filtering or bridging application, the MU9C8338 parses incoming frames for both the source address (SA) and the destination address (DA). It then automatically performs all the address table lookup functions required to allow the control hardware to make the correct forwarding decision. Time stamps are added or updated automatically during the address table lookups, which removes the need for additional management software. A group of built-in routines enables the system to purge older entries from the database, adjust the time stamps, and add and remove permanent entries when required.

This Application Note describes how the MU9C8338 can accelerate single-port Ethernet address filtering functions as one would see in a Wireless LAN (WLAN) application. The device functionality is described in detail with emphasis given to the input and output signals required when transferring data. Software and hardware examples are provided to show how a MU9C8338 device is configured and used in a typical application. Figure 1 shows the block diagram of a typical application utilizing a MU9C8338 device.

FUNCTIONAL DESCRIPTION

The MU9C8338 is used in single-port Ethernet bridging and filtering applications to extract and process the address information from incoming packets. After parsing the DA and SA, the MU9C8338 provides the appropriate information so that the packet is appropriately handled. In order to make this decision, the MU9C8338 compares the DA with a table of addresses stored in an external CAM. After the comparison is performed, the result is available to the surrounding hardware through a result output port or by reading an internal software register. If the comparison yields a match, the device either Rejects or Accepts the packet depending on the configuration registers setting.

The MU9C8338 also compares the SA of the received packet. If it is not found, then it is added to the table along with the port identification (PortID is user defined, default = 000000b). If a match is found, the port number is updated in order to keep the address database accurate. An 8-bit time stamp value is also automatically added to the table entries as they are added or updated. This allows the system to delete older entries at regular intervals in order to remove address information that is no longer valid. The host CPU has full control over the time stamping mechanism to adjust the time that entries stay in the database. This allows increased entry life when network traffic is low and decreased when network traffic is high. The routine that purges entries can be invoked by asserting a hardware pin or by writing to a software register.

In a device configuration shown in Figure 1, the MU9C8338 and its associated CAM is initialized and configured by the host CPU to perform all the DA and SA filter operations automatically as each packet is received. As each packet is processed, the MU9C8338 indicates that the result is available by asserting a result port hardware pin. An optional interrupt also can be sent to the host processor if required. The result is read by external hardware through a result port or by the CPU by checking an internal register.

The MU9C8338 also has other built-in routines that allow simple management tasks. The included routines allow the following:

- Permanent entries can be added/removed
- Entries can be read out
- Older entries can be purged

The host CPU selects the routines by writing to the appropriate 16-bit System Command register.

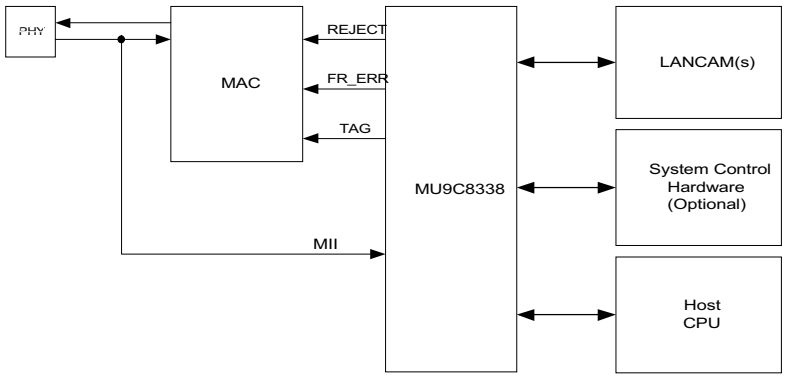

Figure 1: Typical Single-Port System

HARDWARE IMPLEMENTATION

The MU9C8338 has the following five distinct interface ports for transferring data to/from the device:

- Processor port
- Result port
- LANCAM Interface
- JTAG Test Access Port
- IEEE 802.3 Standard Media Independent Interface (MII) and Tag port

This section explains how the interface port should be configured when the device is used to facilitate a single-port address filter.

Processor Port

The Processor port transfers data to and from the MU9C8338's three internal register sets. This allows the host CPU to initialize and configure both the internal registers and the LANCAM database and perform general system management and maintenance tasks. When configuring the LANCAMs, they are not accessed directly by the host processor. Commands are written to the LANCAM Control Signals (SLCCS) and CAM Data Word 0 (SCDW0) register allowing the proper LANCAM configuration. When configuration is completed, the general system tasks are also performed through the Processor port by writing to the appropriate System Command register. The tasks include initiating any of the built-in routines and other general management duties.

The Processor port consists of a 16-bit data bus (D[15:0]), 8-bit address bus (A[7:0]) and the associated signals required for successful data transfer. The MU9C8338 has three sets of internal registers that are accessed by loading the appropriate address on A[7:0] while asserting the required chip select. /PCSS is the Processor Chip Select System and must be asserted LOW to access the 23 System registers. /PCS is the Processor Chip Select and must be asserted LOW to access the four Chip registers and the four Port registers in each device.

/WRITE Input

The /WRITE input determines the direction of data flow into or out of the processor port. If it is LOW, the data placed on D[15:0] is written to the specified register. On the other hand, if it is HIGH, the contents of the required register is placed on D[15:0] by the device. PROC_RDY is a tri-state output from the MU9C8338 that ensures successful data transfer. When reading from or writing to the internal registers, the MU9C8338 asserts PROC_RDY to indicate that the data was received or the data was placed on the bus.

/INTR Output

The /INTR output indicates an interrupt to the host CPU. The user configures whether certain events cause an interrupt by setting the appropriate bits in the System and Port Target registers. An interrupt service routine should respond to an interrupt by checking each register in turn until the cause is found. For a detailed description of each signal and for the required timing specifications, please refer to the MU9C8338 Data Sheet. Interrupt configurations are described below.

Result Data Available

When the MU9C8338 has processed a packet's DA and the result is available, the Result Status (RSTAT) register must be read to determine if there is result data available. The data can be read by accessing the Result Data (RDAT) register. A subsequent RDAT register read returns the next result. When one result has been read, any interrupt service routine should read RSTAT again to confirm if there is any further data to be read. The /INTR pin returns to its normal state when all the result data has been read. Alternatively, the result data can be accessed directly through the hardware result port.

Note: *If the Result port is used to access the data, it is recommended that the result interrupt not be configured. Instead, the RP_DV output should be monitored by external hardware to detect when result data is available.*

LANCAM Full

The LANCAM is full. The /INTR pin is returned to normal state when the System Status (SSTAT) register is read and an entry has been removed from the LANCAM. The built-in purge routine can be invoked until the LANCAM Full condition is no longer true.

Result Port

When the MU9C8338 is configured correctly, it parses incoming frames to extract the DA and SA. It automatically performs the required LANCAM database processing functions so that the hardware can handle the packet appropriately. The Result Port is the 19-bit interface that allows the MU9C8338 to communicate the DA search results. RP[15:0] is the 16-bit output that transfers the result data to the surrounding hardware. The result information that is available after each incoming packet has been parsed and analyzed is shown in Table 1. This data is also available to the host CPU by reading the internal RDAT register. The RDAT register bit mapping is identical to the data available through the result port.

It is important to note that although the result data is available through the Result Port and the Processor Port, the source is mutually exclusive. Therefore, any data read from the Result Port is not also transferred to the RDAT register. In the same way, if the user uses the RDAT register to access the data, the Result Port should not be used to ensure all data reaches the register.

From the result information, the incoming packets can be rejected or forwarded. Three control signals are required to read the results as each incoming packet is processed. The MU9C8338 indicates that there is result data by asserting RP_DV HIGH. The RP_NXT, and RP_SEL inputs are used to transfer the data to the surrounding hardware.

RP_DV remains HIGH while there is valid result data available at the 16-bit RP[15:0] output. RP_NXT and RP_SEL control transferring valid data to the interface hardware. RP_SEL is the result port tri-state control and loads the RP[15:0] with the data when it is asserted HIGH. This input can be held HIGH if required.

RP_NXT is asserted HIGH to clock out the next result from RP[15:0] (RP_SEL must also be HIGH). If there is further result data to be read, RP_DV continues to remain HIGH 140ns after RP_NXT is asserted. If there is no further data, RP_DV goes LOW 140 ns after RP_NXT is asserted. When the RDAT register is read through the Processor Port in order to read results, RP_SEL and RP_NXT should remain LOW. This ensures that all the valid data reaches the register. For a detailed description of each signal and for the required timing specifications, please refer to the MU9C8338 Data Sheet.

Table 1: Result Port Bit Descriptions

Bit(s)	Description
15:10	Source Port ID: Default = (00h).
9:8	Packet Type. This indicates if the packet that was processed was a broadcast (00), multicast (01), or unicast (10) packet.
7	Match Found. If the processed packet was unicast, this bit indicates whether a match was found during the destination address lookup. This bit is logic 1 for a match and logic 0 for no match.
6:1	Destination Port ID. If there was a match found (bit 7 = 1), these bits indicate the Destination Port. The default is 00h.
0	Destination Port = Source Port. This bit indicates (if a DA match was found) that the packet source was the same as the packet destination, indicating there is no need to forward this packet.

LANCAM Interface

The MU9C8338 can be used with either the LIST XL or LANCAM B family of devices. The MU9C8338 LANCAM Interface consists of signals DQ[15:0], /E, /W, /CM, /EC (not used in LIST XL), /RESET_LC, /MI, and /FI. These are connected directly to the LANCAM devices used to store the address database. When the MU9C8338 has to perform any operations on the LANCAMs, it loads these outputs with the appropriate signal values. LANCAMs (except the LIST XL) can be cascaded to increase address table depth. The LANCAM interface timing can accommodate up to four cascaded LANCAMs. A block diagram showing the LANCAM interface connections for a cascaded LANCAM configuration is shown in Figure 2. The connections for a LIST XL application are shown in Figure 3.

If fewer than four LANCAMs are required, Figure 2 is amended by removing the lowest-priority device(s) (LANCAM 0 is the highest-priority device) and the connected inputs. Connect the /FF and /MF outputs from the new lowest-priority device to the /FI and /MI inputs of

the MU9C8338. If the system address table depth requires more than four cascaded LANCAMs, an external prioritization method can be used. When using this method, care must be taken to ensure that the flag-ripple timing requirements are satisfied. The appropriate LANCAM data sheet gives a full description of how LANCAMs can be cascaded using each method.

The MU9C8338 loads /E, /W, /CM, /EC, and DQ[15:0] with the appropriate signal values to perform all the necessary LANCAM operations. The /FI and /MI inputs indicate the match and full status of the database and are connected to only the last LANCAM's /FF and /MF outputs. /RESET_LC is the reset output from the MU9C8338 and is used to reset the LANCAMs. This output is asserted LOW when the system reset input (/RESET) is also asserted LOW (it remains LOW after /RESET is taken HIGH). Bit [0] of the System Dynamic Configuration register (SDCFG) must be set to logic 1 to return /RESET_LC HIGH to allow normal LANCAMs operation.

MII and Tag Ports

The MU9C8338 has an independent IEEE 802.3 Standard 10/100Mb MII port that receives incoming packets and parses them for address information. Typically the MII bus is "tapped" to collect packet data as it is passed from the PHY to the MAC. When the MII port receives the data, the MU9C8338 automatically extracts the source and destination addresses, performs the appropriate LANCAM lookups, and outputs the result.

The MU9C8338 also provides a Tag Port that communicates the destination port ID when the LANCAM lookups have been completed. This allows MAC devices that support Tag switching to attach the destination port ID to the packet before it is routed through the switch fabric. The Tag port also indicates if incoming packets should be rejected if the destination port ID was identical to the source port ID. If Tag switching is not supported or implemented, these outputs may be left unconnected. The connections are shown in Figure 4.

JTAG Test Access Port

The MU9C8338 has an IEEE 1149.1 compliant JTAG Boundary Scan test access port interface. A serial input bit stream is applied to the TMS input to select the specific boundary scan test. Table 2 shows the test modes that are possible when using the Test Access port. The test data is applied to the internal architecture through the TDI input. The TDO output provides the output path for the test data. TCK is the test clock input and can operate at a frequency up to 10MHz. When the test mode is not being used this input should be tied to a valid logic level. Finally, the /TRST input is the reset input for the test access port. This normally should be connected to the /RESET input or must be held at a LOW logic level when the JTAG port is not being used. /TRST, TMS, and TDI have an internal pull up resistor (25K minimum). Please refer to the IEEE 1149.1 Standard for more information on using the JTAG functions.

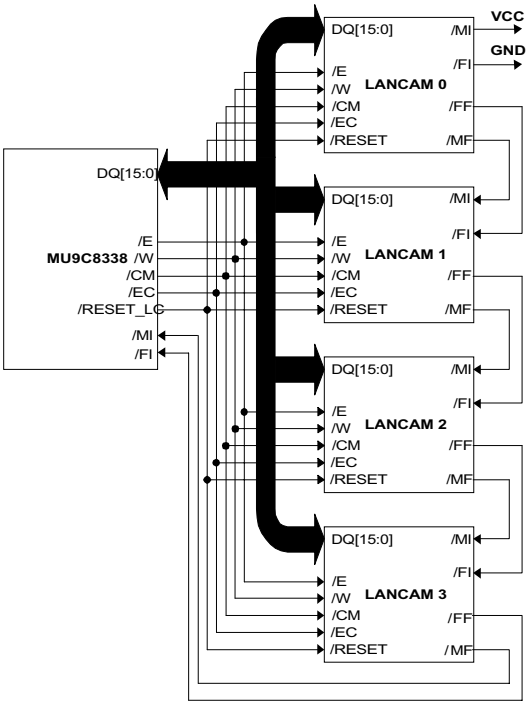

Figure 2: MU9C8338 with Cascaded LANCAMs

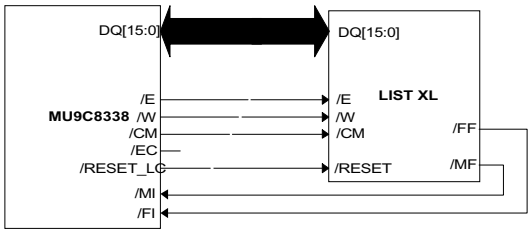

Figure 3: MU9C8338 with LIST XL

Additional Control Pins

The remaining control pins in the MU9C8338 are /RESET, INCR, and SYSCLK. /RESET is the main system reset input. This should be asserted LOW to perform a hardware reset. Before system initialization, and configuration is begun to program the necessary registers, /RESET must be asserted LOW as shown in the System Configuration section.

The INCR input is the hardware purge control and is asserted HIGH. If this bit is enabled in the System Target register, asserting it cause the following to occur:

1. Both the STCURR and STPURG registers are incremented. The new value of STCURR is the 8-bit time stamp value that is added to LANCAM entries between this present time and the next INCR assertion.
2. The time stamps of each entry in the LANCAM database are compared with the new value of STPURG. All matching nonpermanent entries are deleted.

This pin is asserted periodically to remove the older entries from the database to ensure the accuracy of the port ID information. Writing to the SDO_INCTSPR register can also perform this operation. For more detail, refer to Miscellaneous LANCAM Operations on page 13.

The SYSCLK input is the main system clock input and its frequency must be between 20 and 50MHz, inclusive.

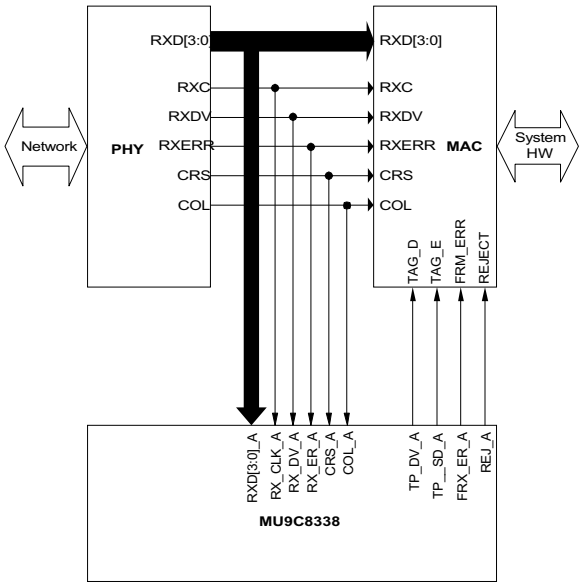

Figure 4: Connections for the MII and Tag Port

SOFTWARE INITIALIZATION AND CONFIGURATION

The MU9C8338 is designed to provide the user with a high performance, large capacity Ethernet processing subsystem. MUSIC LIST XL or LANCAM B Family of devices must be used to store the address table (MAC addresses and associated Port IDs). After configuration, the MU9C8338 performs all the operations required to provide the surrounding hardware with the necessary forwarding information. The MU9C8338 contains a number of built-in routines that allow the user to manually perform certain table management tasks. A group of System Command registers invoke the appropriate routines after the appropriate information are loaded into the CAM Data registers. These are explained in detail in the General LANCAM Housekeeping section. This section describes the following:

- LANCAM or LIST XL device configuration for use in a typical single-port filter or bridge application
- LANCAM configuration using a MU9C8338 System register to control the LANCAM interface port
- Initializing and configuring the MU9C8338 registers and configuring the LANCAMs used as the address database

LANCAM Configuration

The first operation that must be performed before the system operates properly is configuration. The MU9C8338 and the LANCAMs must both be configured to perform all the functions. LANCAM initialization and configuration involves setting the internal control registers with the operating conditions required in the application. For example, the control registers are set to allow the LANCAMs to store 48-bit MAC addresses and return useful associated data in the remaining 16-bit segment.

The MUSIC LANCAM B Family has two sets of control registers that are known as the Foreground and Background Register sets. The Foreground registers are used when performing normal bridging functions such as SA and DA lookups. The Background registers are used when performing the address table management tasks such as purging of older entries, setting the Address register and reading out entries. Table 3 shows how the LANCAM devices is configured in a typical application.

Normally, individual commands are given to any LANCAM device by loading the signal inputs (DQ[15:0], /E, /CM, /EC, /W) with the appropriate values. The /E input to the LANCAM is the main enable input. It is asserted LOW to register the data and other control signals and returned HIGH to complete the cycle. Because the LANCAMs are connected directly to the MU9C8338 using the LANCAM interface, all these signal values are supplied by the MU9C8338.

To allow the user to configure the LANCAMs, direct access is gained by setting bit [4] of the 16-bit System LANCAM Control Signals (SLCCS) register to logic level 1 while setting the other bits to the appropriate values. When using MUSIC LANCAMs, instructions are given or data is written to the device using the DQ[15:0] input/output pins. The control signals (/E, /CM, /EC, /W) are used to complete the data transfer cycle. Four cycles are possible: data write, data read, command write, and command read. The timing specifications that are required and a full description of all LANCAM functions can be found in the appropriate LANCAM B Family Data Sheet.

Table 2: JTAG Codes

Function	Code
EXT TEST	0000
BYPASS	1111
SAMPLE	0001
ID CODE	0010
CLAMP	0100
HIGH-Z	0011
INTEST	0101

The user should access the LANCAMs using the SLCCS register only during configuration. After configuration is complete, Bit 4 of the SLCCS register should be set to logic level 0. There is no need to access the LANCAM after configuration using this register. Built-in routines have been included that allow general LANCAM housekeeping operations (refer to Miscellaneous LANCAM Operations on page 13). When the user has control of the LANCAMs to read or write, the control outputs are manipulated by writing values to the SLCCS register.

Table 4 shows the register bit assignments that are required for each cycle used during configuration. Please note that a command read cycle is required only during initialization and configuration to clear up any power-up anomalies in the LANCAMs. To complete a LANCAM cycle during configuration, four distinct chronological steps must be followed to transfer data successfully to the LANCAMs. Table 5 shows the four steps that are required for each cycle. When performing the command read cycle that is required to clear power-up anomalies, step 1 is omitted.

Table 3: Typical Application Foreground and Background Register Settings

Register	Register Set	Description
Page Address	Shared	The Page address register of each device is set as follows: 1st device PA = 0, 2nd device PA=1, 3rd device PA=2, 4th device PA=3. ***Note:*** *Only the first device PA is defined in single LANCAM applications.*
Control	Foreground	Set for 48 bits CAM, 16 bits RAM, the compares do not use a Mask Register, Enhanced Mode, the Address register increments.
Segment Control	Foreground	Set for writes to segments 3:0 and reads from segment 0 only.
Mask 1	Foreground	Segment 3=0000h, Segment 2=0000h, Segment1=0000h, segment 0=8000h. This is to mask the permanent bit in order to update only the PortID and time stamp during the automatic SA filter routine.
Persistent Destination	Foreground	This is set as Comparand Register.
Persistent Source	Foreground	This is set as Highest Match.
Control	Background	Set for 64 bits CAM, 0 bits RAM, the compares use Mask Register1, Enhanced Mode, the Address register increments.
Segment Control	Background	Set for writes to segment 0 only and reads from segment 3:0.
Mask 1	Background	Segment 3=FFFFh, segment 2=FFFFh, segment 1=FFFFh, segment 0=7F00h.This is to mask the PortID in order to perform the purge routine.
Persistent Destination	Background	This is set as the Comparand Register.
Persistent Source	Background	This is set as the memory location that is specified by the Address Register.

Table 4: SLCCS Register Bit Assignments

Bit 4 CAM Access	Bit 3 /E	Bit 2 /W	Bit 1 /CM	Bit 0 /EC	16-bit SLCCS	Cycle
0	1	1	1	1	0Fh	The user has no direct access to the LANCAMs
1	1	0	0	1	19h	Command write with daisy chain locked (/E high)
1	0	0	0	1	11h	Command write with daisy chain locked (/E low)
1	1	1	0	1	1Dh	Command read with daisy chain locked (/E high)
1	0	1	0	1	15h	Command read with daisy chain locked (/E low)
1	1	0	1	1	1Bh	Data write with daisy chain locked (/E high)
1	0	0	1	1	13h	Data write with daisy chain locked (/E low)

Table 5: LANCAM Configuration Cycle Steps

Step	Register	Description
1	SCDW0	Write the Op-Code (command cycle) or the data to be transferred (data cycle) to the System CAM Data Word 0 (SCDW0) register. The MU9C8338 loads the DQ[15:0] pins of the LANCAM interface with the contents of this register during the cycle.
2	SLCCS	Write the appropriate value from Table 4 to the SLCCS register that sets up the LANCAM interface control outputs. This is the value that has /E set HIGH (e.g., 19h if it is a command write cycle).
3	SLCCS	Write the appropriate value from Table 4 to the SLCCS register that begins the data transfer by asserting /E LOW (e.g., 11h if it is a command write cycle).
4	SLCCS	Write the appropriate value from Table 4 to the SLCCS register that completes the data transfer by returning /E HIGH (e.g., 19h if it is a command write cycle).

System Configuration

After power-up or hardware reset, the host processor must perform the system initialization and configuration sequence. This involves setting the MU9C8338 System, Chip and Port registers to the values that are required for a typical single-port filter application. The LANCAM devices are initialized and configured as described in Software Initialization and Configuration on page 5. The following reset sequence must take place in the order specified before the host processor performs the configuration sequence:

1. While /RESET is HIGH, RP_NXT must be held HIGH.
2. While /RESET is HIGH, RP_SEL must be held LOW.
3. While /RESET is HIGH, INCR must be held LOW.
4. /RESET is asserted LOW for a minimum of 1 ms and then returned HIGH.
5. RP_NXT, RP_SEL, and INCR may be set to any appropriate valid level.

Table 6 shows the configuration sequence in full. The following configuration sequence assumes four cascaded MUSIC LANCAMs. The host CPU writes the values shown to the appropriate registers. /PCS is asserted, after address decoding, when the Port or Chip registers are the targets. Similarly, /PCSS is asserted after address decoding, when the System registers are the targets. The configuration sequence is described as follows:

Line 1 configures the MU9C8338 as the MASTER device and sets its CHIPROL register to 00H (MASTER device). Line 2 sets the System Static Configuration register for 90 ns LANCAMs and sets the port REJ output as active LOW. Line 3 sets the System DA/SA Cycle register to accommodate the 90 ns LANCAMs selected in line 2. Line 4 sets the System Dynamic Configuration register to enable the LANCAM devices. This takes the /RESET_LC output in the LANCAM interface HIGH allowing the LANCAMs to function normally.

Line 5 sets the Port ID as 00H. It is important to note that the Port Configuration (PCFG) register has a default setting of 00H, which disables the 10 Base-X CRC facility. The configuration in this application note does not require the CRC facility, therefore, the PCFG register is left with default settings. If this facility is to be enabled in the users specific application, it is recommended that it be performed between lines 5 and 6.

Lines 6 through 179 initialize and configure the four LANCAMs to operate properly with the built-in LANCAM system routines. Lines 6 and 7 set the System LANCAM Control Signals register to 0FH for two cycles.

This is to ensure that the LANCAM interface outputs are in a safe mode before direct access to the LANCAM is enabled. Line 8 presets the LANCAM interface to the values required for a command read cycle before direct access is selected. The subsequent LANCAM cycles in this explanation are the type described in detail in the LANCAM configuration section. Lines 9 through 11 perform a LANCAM command read cycle to ensure that any anomalies residing in the LANCAMs after power up are removed before configuration begins. Lines 12 through 19 set the Device Select register to FFFFH to ensure all the LANCAMs respond to subsequent commands. Lines 20 through 27 reset all the LANCAMs by setting the Control registers to 0000H.

Lines 28 through 79 set the Page Address registers of the four LANCAM devices as 00H, 01H, 02H, and 03H. This is done as follows: Lines 28 through 31 targets the Page Address register of the highest-priority (lowest address) device in the chain of four LANCAMs. Lines 32 through 35 set the value of the Page Address register as 00H. Lines 36 through 39 sets the Full flag on this device forcing the next device in the chain to respond to the next set of initialization commands. Lines 40 through 47 targets the highest-priority device again (which is now the second device) and sets the Page Address value as 01H. Lines 48 through 71 continue to set the Full flag of each device and set the page address of the next device until the last device is set. The last device does not require its Full flag to be set as there are no lower priority devices remaining. Lines 72 through 79 perform a reset forcing the Full flag of all the devices in the chain to their normal function. This reset leaves the recently configured Page Address values unaffected. In most single-port applications, such as a WLAN access point, a single LANCAM provides adequate depth. If only one LANCAM is in use, omit lines 36 through 79. If two are used, omit lines 45 through 71 and if three are used, omit lines 60 through 71.

Lines 80 through 127 set the Background registers for use in the purge, set Address register and read entries routines. This is done as follows: Lines 80 through 83 select the Background Register set. Lines 84 through 91 set the Control register to operate with the CAM/RAM partition set for 64 bits of CAM and 0 bits of RAM. It is also set to use Mask Register 1 when doing any comparisons, operate in Enhanced mode, and increment the Address register. Lines 92 through 95 set the persistent destination of subsequent data writes as Mask register 1. Lines 96 through 111 set the Mask register as segment 0 = 7F00H, segment 1 = FFFFH, segment 2 = FFFFH, and segment 3 = FFFFH. This ensures that only the permanent bit and time stamp bits are compared during comparisons using the Background Register set.

Lines 112 through 119 set the Segment Control register as follows: When data is written to the LANCAMs, it is received only in segment 0. When data is read from the LANCAMs, it is read from segments 0 through 3. Lines 120 through 127 set the persistent source and destination for any future data reads and writes. The Comparand register receives any data written to the LANCAMs. The memory location specified by the Address register are the source for any future data that is read from the LANCAMs.

Lines 128 through 175 set the Foreground registers for use in the normal DA and SA filtering routines and for the addition and deletion of permanent entries. This is done as follows: Lines 128 through 131 select the Foreground register set. Lines 132 through 139 set the Control register to operate with the CAM/RAM partition set for 48 bits of CAM and 16 bits of RAM. It also is set not to use any Mask registers when doing comparisons, operate in Enhanced mode, and increment the Address register. Lines 140 through 147 set the Segment Control register as follows: When data is written to the LANCAMs, it is received in segments 0 through 3. When data is read from the LANCAMs, it is only read from segment 0. Lines 148 through 151 set the persistent destination of subsequent data writes as Mask register 1. Lines 152 through 167 set the Mask register as segment 0 = 8000H, segment 1 = 0000H, segment 2 = 0000H, and segment 3 = 0000H. This ensures that the permanent bit is unaltered when the SA filter routine results in MATCH condition.

Lines 168 through 175 set the persistent source and destination for any future data reads and writes. The Comparand register receives any data written to the LANCAMs. The memory location containing the highest-priority match during the DA filter routine is the source for any future data read from the LANCAMs. Lines 176 and 177 set the SLCCS register to 1FH for two cycles. This is to ensure that the LANCAM interface control lines are in a safe state before direct access is turned off. Lines 178 and 179 set the SLCCS register to 0FH for two cycles. This returns control of the LANCAM interface to the MU9C8338. Line 180 sets the System Target register to increment the STPURG and STCURR registers when the INCR input pin is asserted. It is also set to enable an interrupt on the /INTR output whenever the LANCAMs become full (LANCAM /FF asserted LOW).

Line 181 sets the Port Target register to allow the MU9C8338 device to process the SA and DA automatically as they are parsed from incoming packets. The register also is configured to enable an interrupt when each DA is processed.

Table 6: Initialization and Configuration Routine

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description
1	H	L	01H	0000H	CHIPROL	Configure device as master
2	L	H	01H	0003H	SSCFG	Set static configuration as reject output as active LOW. Also set for 90 ns CAMs.
3	L	H	0CH	0025H	SMXSADACYC	Set the DA/SA cycle time for 90 ns CAMs
4	L	H	02H	0001H	SDCFG	Set the System Dynamic Configuration register to enable the LANCAM devices
5	H	L	40H	0000H	PID	Set Port ID for port 0
6	L	H	12H	000FH	SLCCS	Put CAM output lines into safe mode
7	L	H	12H	000FH	SLCCS	Wait
8	L	H	12H	000DH	SLCCS	Preset CAM control lines to initial state
9	L	H	12H	001DH	SLCCS	Set up command read condition to clear up any power up anomalies
10	L	H	12H	0015H	SLCCS	Take /E bit LOW
11	L	H	12H	001DH	SLCCS	Take /E bit HIGH
12	L	H	05H	0228H	SCDW0	Load register with Op-Code: TCO DS
13	L	H	12H	0019H	SLCCS	Set up command write condition
14	L	H	12H	0011H	SLCCS	Take /E bit LOW
15	L	H	12H	0019H	SLCCS	Take /E bit HIGH
16	L	H	05H	FFFFH	SCDW0	Load register with device: FFFFH = all devices
17	L	H	12H	0019H	SLCCS	Set up command write condition
18	L	H	12H	0011H	SLCCS	Take /E bit LOW
19	L	H	12H	0019H	SLCCS	Take /E bit HIGH
20	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT
21	L	H	12H	0019H	SLCCS	Set up command write condition
22	L	H	12H	0011H	SLCCS	Take /E bit LOW
23	L	H	12H	0019H	SLCCS	Take /E bit HIGH
24	L	H	05H	0000H	SCDW0	Load register with code: 0000H=reset all devices
25	L	H	12H	0019H	SLCCS	Set up command write condition
26	L	H	12H	0011H	SLCCS	Take /E bit LOW
27	L	H	12H	0019H	SLCCS	Take /E bit HIGH
28	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA
29	L	H	12H	0019H	SLCCS	Set up command write condition
30	L	H	12H	0011H	SLCCS	Take /E bit LOW
31	L	H	12H	0019H	SLCCS	Take /E bit HIGH
32	L	H	05H	0000H	SCDW0	Load register with code: 0000H = set page address of first device
33	L	H	12H	0019H	SLCCS	Set up command write condition
34	L	H	12H	0011H	SLCCS	Take /E bit LOW
35	L	H	12H	0019H	SLCCS	Take /E bit HIGH
36	L	H	05H	0700H	SCDW0	Load register with Op-Code: SFF
37	L	H	12H	0019H	SLCCS	Set up command write condition
38	L	H	12H	0011H	SLCCS	Take /E bit LOW
39	L	H	12H	0019H	SLCCS	Take /E bit HIGH
40	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA
41	L	H	12H	0019H	SLCCS	Set up command write condition
42	L	H	12H	0011H	SLCCS	Take /E bit LOW
43	L	H	12H	0019H	SLCCS	Take /E bit HIGH
44	L	H	05H	0001H	SCDW0	Load register with code: 0001H = set page address of second device
45	L	H	12H	0019H	SLCCS	Set up command write condition
46	L	H	12H	0011H	SLCCS	Take /E bit LOW
47	L	H	12H	0019H	SLCCS	Take /E bit HIGH

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description
48	L	H	05H	0700H	SCDW0	Load register with Op-Code: SFF
49	L	H	12H	0019H	SLCCS	Set up command write condition
50	L	H	12H	0011H	SLCCS	Take /E bit LOW
51	L	H	12H	0019H	SLCCS	Take /E bit HIGH
52	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA
53	L	H	12H	0019H	SLCCS	Set up command write condition
54	L	H	12H	0011H	SLCCS	Take /E bit LOW
55	L	H	12H	0019H	SLCCS	Take /E bit HIGH
56	L	H	05H	0002H	SCDW0	Load register with code: 0002H = set page address of third device
57	L	H	12H	0019H	SLCCS	Set up command write condition
58	L	H	12H	0011H	SLCCS	Take /E bit LOW
59	L	H	12H	0019H	SLCCS	Take /E bit HIGH
60	L	H	05H	0700H	SCDW0	Load register with Op-Code: SFF
61	L	H	12H	0019H	SLCCS	Set up command write condition
62	L	H	12H	0011H	SLCCS	Take /E bit LOW
63	L	H	12H	0019H	SLCCS	Take /E bit HIGH
64	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA
65	L	H	12H	0019H	SLCCS	Set up command write condition
66	L	H	12H	0011H	SLCCS	Take /E bit LOW
67	L	H	12H	0019H	SLCCS	Take /E bit HIGH
68	L	H	05H	0003H	SCDW0	Load register with code: 0003H = set page address of fourth device
69	L	H	12H	0019H	SLCCS	Set up command write condition
70	L	H	12H	0011H	SLCCS	Take /E bit LOW
71	L	H	12H	0019H	SLCCS	Take /E bit HIGH
72	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT
73	L	H	12H	0019H	SLCCS	Set up command write condition
74	L	H	12H	0011H	SLCCS	Take /E bit LOW
75	L	H	12H	0019H	SLCCS	Take /E bit HIGH
76	L	H	05H	0000H	SCDW0	Load register with code: 0000H = reset all devices to clear full flags
77	L	H	12H	0019H	SLCCS	Set up command write condition
78	L	H	12H	0011H	SLCCS	Take /E bit LOW
79	L	H	12H	0019H	SLCCS	Take /E bit HIGH
80	L	H	05H	0619H	SCDW0	Load register with Op-Code: SBR
81	L	H	12H	0019H	SLCCS	Set up command write condition
82	L	H	12H	0011H	SLCCS	Take /E bit LOW
83	L	H	12H	0019H	SLCCS	Take /E bit HIGH
84	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT
85	L	H	12H	0019H	SLCCS	Set up command write condition
86	L	H	12H	0011H	SLCCS	Take /E bit LOW
87	L	H	12H	0019H	SLCCS	Take /E bit HIGH
88	L	H	05H	8011H	SCDW0	Load register with code: 8011H = 64 bits CAM, 0 bits RAM, use MR1, Enhanced, increment Address register
89	L	H	12H	0019H	SLCCS	Set up command write condition
90	L	H	12H	0011H	SLCCS	Take /E bit LOW
91	L	H	12H	0019H	SLCCS	Take /E bit HIGH
92	L	H	05H	0108H	SCDW0	Load register with Op-Code: SPD MR1
93	L	H	12H	0019H	SLCCS	Set up command write condition
94	L	H	12H	0011H	SLCCS	Take /E bit LOW

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description
95	L	H	12H	0019H	SLCCS	Take /E bit HIGH
96	L	H	05H	7F00H	SCDW0	Load register with code: 7F00H = data write 7F00H to first segment of MR1
97	L	H	12H	001BH	SLCCS	Set up data write condition
98	L	H	12H	0013H	SLCCS	Take /E bit LOW
99	L	H	12H	001BH	SLCCS	Take /E bit HIGH
100	L	H	05H	FFFFH	SCDW0	Load register with code: FFFFH = data write FFFFH to second segment of MR1
101	L	H	12H	001BH	SLCCS	Set up data write condition
102	L	H	12H	0013H	SLCCS	Take /E bit LOW
103	L	H	12H	001BH	SLCCS	Take /E bit HIGH
104	L	H	05H	FFFFH	SCDW0	Load register with code: FFFFH = data write FFFFH to third segment of MR1
105	L	H	12H	001BH	SLCCS	Set up data write condition
106	L	H	12H	0013H	SLCCS	Take /E bit LOW
107	L	H	12H	001BH	SLCCS	Take /E bit HIGH
108	L	H	05H	FFFFH	SCDW0	Load register with code: FFFFH = data write FFFFH to fourth segment of MR1
109	L	H	12H	001BH	SLCCS	Set up data write condition
110	L	H	12H	0013H	SLCCS	Take /E bit LOW
111	L	H	12H	001BH	SLCCS	Take /E bit HIGH
112	L	H	05H	0210H	SCDW0	Load register with Op-Code: TCO SC
113	L	H	12H	0019H	SLCCS	Set up command write condition
114	L	H	12H	0011H	SLCCS	Take /E bit LOW
115	L	H	12H	0019H	SLCCS	Take /E bit HIGH
116	L	H	05H	00C0H	SCDW0	Load register with code: 00C0H = write to segment 0, read from segments 0–3
117	L	H	12H	0019H	SLCCS	Set up command write condition
118	L	H	12H	0011H	SLCCS	Take /E bit LOW
119	L	H	12H	0019H	SLCCS	Take /E bit HIGH
120	L	H	05H	0100H	SCDW0	Load register with Op-Code: SPD CR
121	L	H	12H	0019H	SLCCS	Set up command write condition
122	L	H	12H	0011H	SLCCS	Take /E bit LOW
123	L	H	12H	0019H	SLCCS	Take /E bit HIGH
124	L	H	05H	0004H	SCDW0	Load register with Op-Code: SPS M@[AR]
125	L	H	12H	0019H	SLCCS	Set up command write condition
126	L	H	12H	0011H	SLCCS	Take /E bit LOW
127	L	H	12H	0019H	SLCCS	Take /E bit HIGH
128	L	H	05H	0618H	SCDW0	Load register with Op-Code: SFR
129	L	H	12H	0019H	SLCCS	Set up command write condition
130	L	H	12H	0011H	SLCCS	Take /E bit LOW
131	L	H	12H	0019H	SLCCS	Take /E bit HIGH
132	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT
133	L	H	12H	0019H	SLCCS	Set up command write condition
134	L	H	12H	0011H	SLCCS	Take /E bit LOW
135	L	H	12H	0019H	SLCCS	Take /E bit HIGH
136	L	H	05H	8041H	SCDW0	Load register with code: 8041H = 48 bits CAM, 16 bits RAM, no mask, Enhanced, increment Address register
137	L	H	12H	0019H	SLCCS	Set up command write condition
138	L	H	12H	0011H	SLCCS	Take /E bit LOW
139	L	H	12H	0019H	SLCCS	Take /E bit HIGH

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description
140	L	H	05H	0210H	SCDW0	Load register with Op-Code: TCO SC
141	L	H	12H	0019H	SLCCS	Set up command write condition
142	L	H	12H	0011H	SLCCS	Take /E bit LOW
143	L	H	12H	0019H	SLCCS	Take /E bit HIGH
144	L	H	05H	1800H	SCDW0	Load register with code: 1800H = write to segments 0–3, read from segment 0
145	L	H	12H	0019H	SLCCS	Set up command write condition
146	L	H	12H	0011H	SLCCS	Take /E bit LOW
147	L	H	12H	0019H	SLCCS	Take /E bit HIGH
148	L	H	05H	0108H	SCDW0	Load register with Op-Code: SPD MR1
149	L	H	12H	0019H	SLCCS	Set up command write condition
150	L	H	12H	0011H	SLCCS	Take /E bit LOW
151	L	H	12H	0019H	SLCCS	Take /E bit HIGH
152	L	H	05H	8000H	SCDW0	Load register with code: 8000H = data write to 8000H to first segment of MR1
153	L	H	12H	001BH	SLCCS	Set up data write condition
154	L	H	12H	0013H	SLCCS	Take /E bit LOW
155	L	H	12H	001BH	SLCCS	Take /E bit HIGH
156	L	H	05H	0000H	SCDW0	Load register with code: 0000H = data write 0000H to second segment of MR1
157	L	H	12H	001BH	SLCCS	Set up data write condition
158	L	H	12H	0013H	SLCCS	Take /E bit LOW
159	L	H	12H	001BH	SLCCS	Take /E bit HIGH
160	L	H	05H	0000H	SCDW0	Load register with code: 0000H = data write 0000H to third segment of MR1
161	L	H	12H	001BH	SLCCS	Set up data write condition
162	L	H	12H	0013H	SLCCS	Take /E bit LOW
163	L	H	12H	001BH	SLCCS	Take /E bit HIGH
164	L	H	05H	0000H	SCDW0	Load register with code: 0000H = data write 0000H to fourth segment of MR1
165	L	H	12H	001BH	SLCCS	Set up data write condition
166	L	H	12H	0013H	SLCCS	Take /E bit LOW
167	L	H	12H	001BH	SLCCS	Take /E bit HIGH
168	L	H	05H	0100H	SCDW0	Load register with Op-Code: SPD CR
169	L	H	12H	0019H	SLCCS	Set up command write condition
170	L	H	12H	0011H	SLCCS	Take /E bit LOW
171	L	H	12H	0019H	SLCCS	Take /E bit HIGH
172	L	H	05H	0005H	SCDW0	Load register with Op-Code: SPS HM
173	L	H	12H	0019H	SLCCS	Set up command write condition
174	L	H	12H	0011H	SLCCS	Take /E bit LOW
175	L	H	12H	0019H	SLCCS	Take /E bit HIGH
176	L	H	12H	001FH	SLCCS	Return LANCAM Interface to inactive
177	L	H	12H	001FH	SLCCS	Wait
178	L	H	12H	000FH	SLCCS	Return to Normal
179	L	H	12H	000FH	SLCCS	Wait
180	L	H	03H	000EH	STARG	Configure system targets as: INCR input results in STURR and STPURG increment and a purge. Full Flag produces an Interrupt on /INTR output.
181	H	L	42H	0060H	PTARG	Set Port 0 to process DA, SA, and enable interrupts.

MISCELLANEOUS LANCAM OPERATIONS

This section shows the steps required when the following operations are performed:

- Add permanent entries to the LANCAMs
- Remove permanent entries from the LANCAMs
- Set the Page Address and actual Address of a LANCAM entry and read it from the LANCAMs
- Maintain the Current Time Stamp and Purge Time Stamp counters
- Initiate the purge routine to delete the oldest entries from the LANCAMs

The MU9C8338 has seven System Command registers (SDO_xxx) that allow invoking a set of built-in LANCAM routines. This allows the user to perform LANCAM system management tasks such as adding or removing permanent entries or reading out existing entries. Writing any arbitrary value to the relevant register triggers the routine. Table 7 shows the registers and the built-in routines that they perform. Tables 8 through 14 show how each built-in routine is invoked to perform the general management tasks.

Table 7: System Data Output Registers and Associated Routines

Register	Address	Description of Routine Invoked
SDO_DELETE	20H	Specific MAC addresses may be deleted from the LANCAM database. The user specifies the MAC address by writing it to the SCDW registers, and when triggered, the routine performs a lookup and deletes it.
SDO_ADD	21H	MAC addresses and associated data may be added to the LANCAM database. The user specifies the MAC address by writing it to the SCDW registers, and when triggered, the routine adds it to the next free location in the LANCAM(s).
SDO_READ	24H	Specific MAC addresses may be read from the LANCAM database. The user specifies the LANCAM page address by writing it to SCDW0 and when triggered, the routine returns the 64-bit LANCAM entry and the status information associated with it. The set address (SDO_SETADD) routine must be used prior to this routine being invoked, to specify the LANCAM address.
SDO_INCTS	26H	The Current Time Stamp counter may be incremented using the routine invoked by SDO_INCTS. This allows increasing the value in the register to the value that suits the present network traffic.
SDO_INCPR	27H	The Purge Time Stamp counter may be incremented using the routine invoked by SDO_INCPR. When this routine is invoked, the new Purge Time Stamp counter value is compared with the MAC addresses time stamps stored in the LANCAM database. All entries that have matching time stamps are deleted. This allows increasing the value in the register to the value that suits the present network traffic.
SDO_INCTSPR	28H	The Current Time Stamp and Purge Time Stamp counters may both be incremented using the routine invoked by SDO_INCTSPR. When this routine is invoked, the new Purge Time Stamp counter value is compared with the MAC addresses time stamps stored in the LANCAM database. All entries that have matching time stamps are deleted.
SDO_SETADD	29H	The LANCAM database Address register may be set to a specific value. This is done prior to the read entry (SDO_READ) routine being invoked.

48-Bit MAC Address Storage

The two built-in routines that write and delete MAC addresses require the MAC address bits to be arranged in a specific manner. For example, the MAC address 02:60:8C:12:34:56 would be written to the SCDW registers as follows when interpreting Table 8 and Table 9.

SA bits [47:40] = 02
SA bits [39:32] = 60
SA bits [31:24] = 8C
SA bits [23:16] = 12
SA bits [15:8] = 34
SA bits [7:0] = 56

Similarly, when using the appropriate built-in routine to read an entry, Table 9 should be interpreted in the same manner. For example, if the MAC address 02:60:8C:12:34:56 is read from the LANCAM, the 3 16-bit words would be as follows:

CAM seg. 3 = 6002
CAM seg. 2 = 128C
CAM seg. 1 = 5634

Add Permanent Entry

During normal system operation, the MU9C8338 parses incoming packets and automatically adds the SAs and their port ID to the LANCAM database. Permanent entries may be added to the LANCAMs manually by invoking a built-in routine as described in Table 8. This is done as follows: Line 1 loads the System CAM Data Word 3 (SCDW3) register with bits [47:32] of the permanent MAC address to be added. Lines 2 and 3 load the remaining MAC address bits into the appropriate SCDW registers. Line 4 loads SCDW0 with the appropriate associated data. This includes the Port ID at bits [13:8] and bit [15] set to 1 to indicate a permanent entry. Line 5 triggers the built-in routine by loading the SDO_ADD register with any 16-bit value. When this register is accessed, the MU9C8338 invokes a routine that takes the contents of the SCDW registers and adds them to the next free LANCAM database location. The entry is not removed from the database by the periodical purging of older entries and must be removed manually when necessary.

Table 8: Adding Permenant Entries Using the Built-In Routine

Line	/PCSS	/WRITE	A[7:0]	D[15:8]	D[7:0]	Register	Description	Note
1	L	L	08H	SA bits [39:32]	SA bits [47:40]	SCDW3	Load register with address bits 47–32	
2	L	L	07H	SA bits [23:16]	SA bits [31:24]	SCDW2	Load register with address bits 31–16	
3	L	L	06H	SA bits [7:0]	SA bits [15:8]	SCDW1	Load register with address bits 15–0	
4	L	L	05H	aaH	aaH	SCDW0	Load register with associated data	1
5	L	L	21H	xxH	xxH	SDO_ADD	Trigger the add entry routine	2

Notes:

1. *aa = The associated data of the MAC address. This has bit 15 set to 1 to indicate a permanent entry and bits 13–8 set to indicate the Port ID.*
2. *xx = "Don't care"*

Delete Permanent Entries

Permanent entries are not removed by the MU9C8338 when the LANCAM database contents are periodically purged to remove older entries. Permanent entries must be removed by invoking the delete entries routine as shown in Table 9. Line 1 loads the System CAM Data Word 2 (SCDW2) register with bits [47:32] of the permanent MAC address to be deleted. Lines 2 and 3 load the remaining MAC address bits into the appropriate SCDW registers. Line 4 triggers the built-in routine by loading the SDO_DELETE register with any 16-bit value. When this register is accessed, the MU9C8338 invokes a routine that takes the SCDW registers contents and compares the 48-bit MAC address with the LANCAM database contents. The matching entry is deleted.

Table 9: Deleting Permenant Entries Using the Built-In Routine

Line	/PCSS	/WRITE	A[7:0]	D[15:8]	D[7:0]	Register	Description	Note
1	L	L	07H	SA bits [39:32]	SA bits [47:40]	SCDW2	Load register with address bits 47–32	
2	L	L	06H	SA bits [23:16]	SA bits [31:24]	SCDW1	Load register with address bits 31–16	
3	L	L	05H	SA bits [7:0]	SA bits [15:8]	SCDW0	Load register with address bits 15–0	
4	L	L	20H	xxH	xxH	SDO_DELETE	Trigger the delete entry routine	1

Notes:

xx = "Don't care"

Reading LANCAM Entries

The user may wish to keep track of the active addresses stored in the LANCAM database. The system would have to read out entries periodically and store them in a shadow table in the normal system memory. It also may be required to investigate the LANCAM entries to locate information such as a specific Port ID of a known MAC address. To allow the LANCAM entries to be read out, two built-in routines have been provided. When used together in the manner specified, they set the page address and physical address of the entry and then read the entry and status information. The page address provides the identity of an individual LANCAM if more than one is used in the LANCAM database.

Table 10 shows how the two routines are invoked, and is described as follows: Line 1 loads the SCDW0 register with the physical address of the LANCAM entry to be read. Line 2 triggers the built-in routine by loading the SDO_SETADD register with any 16-bit value. When this register is accessed, the MU9C8338 invokes a routine that takes the SCDW0 register contents and transfers it to the Address register of the LANCAM Background Register set. When the read entry routine is triggered, the entry that is read is the one specified by the Address register.

Line 3 loads the SCDW0 register with the page address of the LANCAM to be read. This specifies the actual LANCAM device to be selected when a chain of multiple devices are used. The value loaded into the SCDW0 register is one of the values configured during the Configuration routine. If only one LANCAM is used, the page address should be 00H. Line 4 triggers the built-in routine by loading the SDO_READ register with any 16-bit value. When this register is accessed, the MU9C8338 invokes a routine that takes the SCDW0 register contents and transfers it to the LANCAM Page Address register. The 64-bit entry specified by the LANCAM Address and Page Address registers is transferred to the MU9C8338 SCDW registers. The 32-bit LANCAM Status register is transferred to the MU9C8338 SCSWA and SCSWB registers.

Lines 5 through 8 read the specified LANCAM entry from the SCDW registers. Lines 9 through 10 read the LANCAM status bits from the SCSWA and SCSWB registers. The 32-bit Status Register value indicates the validity of the entry in bits [29:28]. If this information is the only required status detail, line 10 may be omitted. Please refer to the appropriate LANCAM Family Data Sheet for a full description of the status bits. If a block of entries and their status are to be read sequentially, lines 3 through 10 may be repeated until all the entries have been read. Lines 1 and 2 do not have to be repeated for each entry as the LANCAM Address register automatically increments.

Table 10: Reading Permanent Entries Using the Built-In Routine

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	05H	CAM address	SCDW0	Load register with address of entry	
2	L	L	29H	xxxxH	SDO_SET ADD	Trigger the set address routine	1
3	L	L	05H	Page address	SCDW0	Load register with page address of entry	
4	L	L	24H	xxxxH	SDO_READ	Trigger the read entry routine	1
5	L	H	08H	CAM seg. 3	SCDW3	Read the specified LANCAM entry, bits [63:48], from SCDW3	
6	L	H	07H	CAM seg. 2	SCDW2	Read the specified LANCAM entry, bits [47:32], from SCDW2	
7	L	H	06H	CAM seg. 1	SCDW1	Read the specified LANCAM entry, bits [31:16], from SCDW1	
8	L	H	05H	CAM seg. 0	SCDW0	Read the specified LANCAM entry, bits [15:0], from SCDW0	
9	L	H	0DH	Status bits [31:16]	SCSWB	Read the LANCAM status bits [31:16] from SCSWB	
10	L	H	0EH	Status bits [15:0]	SCSWA	Read the LANCAM status bits [15:0] from SCSWA	

Notes:

1. xxxx = Don't care

Purge Older Entries

The MU9C8338 has two counters that are used when adding time stamps and removing older entries. The first of these counters is the Current Time Stamp counter (STCURR). This 8-bit counter provides 256 possible time stamp values that are added to the associated data field during the SA lookup operation. When the SA lookup routine is performed by the MU9C8338, the 8-bit value of STCURR is automatically added to bits [7:0] of the LANCAM associated data field (bits [15:0]). The second of these counters is the Purge Time Stamp counter (STPURG). This 8-bit counter stores the present purge value. When a purge routine is initiated, this counter is incremented. The value in it is then compared with the 8-bit time stamp value stored with every nonpermanent entry in the LANCAM database. Matching entries are subsequently deleted and purged or aged out.

For example, Figure 5 shows some possible settings of both STCURR and STPURG.

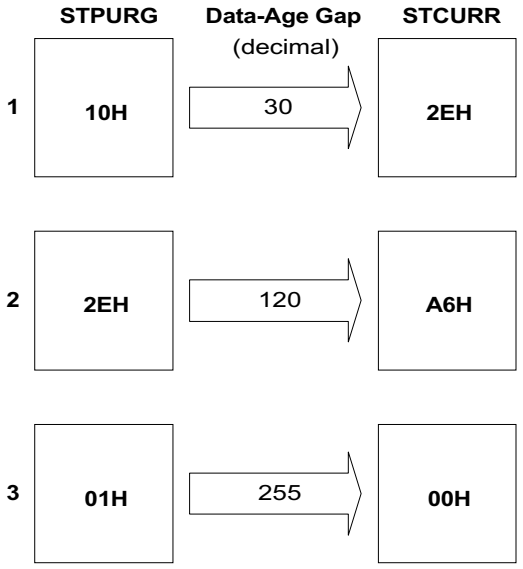

Figure 5: STCURR/STPURG Setting Examples

Item 1 shows both counters set for a very small data-age gap. An entry would exist in the database for 30 purge intervals only, if it were not updated before its time stamp equals STPURG. Item 2 shows a medium data-age gap of 120 and item 3 shows the maximum gap, which is 255. Using item 2 as an example, the purge sequence operates as follows:

1. After a purge of older entries is triggered, both counters are incremented, making STPURG = 2FH and STCURR = A7H. During the time interval between now and when the next purge is triggered, all the time stamps that are added or updated equal A7H.
2. The new value of STPURG (2FH) is compared with all the entries in the LANCAM database. All the entries with the same value as STPURG and not marked as permanent are deleted. If the data-age gap remains constant, any entries added to the database remain undeleted for at least 120 purges.

Built-In Routines

Three built-routines (as shown in Tables 11 through 14) are provided to adjust the counter values and to initiate the purge sequence.

Increment Time Stamp Routine

The first of these routines is the increment time stamp routine and is triggered by writing to the SDO_INCTS register. This adjusts STCURR by adding one to the present value to increase the time entries exist in the LANCAM database. Because STCURR and the STPURG are both 8 bits wide, 256 possible time stamps are possible. By incrementing STCURR, the difference between it and STPURG can be increased, thereby increasing the data-age gap from between 1 and 255 purge intervals. A purge interval is the time interval between the CPU initiating its regular purge of older entries.

Increment Purge Time Stamp Routine

The second routine is the increment purge time stamp routine and is triggered by writing to the SDO_INCPR register. This adjusts STPURG by adding one to the present value and then comparing the new value with bits [7:0] of each nonpermanent entry in the LANCAM database. Matching entries are deleted and removed from the database. By incrementing STPURG, the difference between it and STCURR can be decreased, thereby decreasing the time that entries in the LANCAM database exist.

The SDO_INCTS and SDO_INCPR routines should be used to adjust STCURR and STPURG, thereby adjusting the data-aging rate. By monitoring network traffic density, the difference between the two counters can be increased or decreased to suit. As traffic flow decreases, increasing STCURR (as shown in Table 11) can increase the difference between the counters. This ensures that entries are aged out less frequently. Conversely as traffic flow increases, increasing STPURG (as shown in Table 12) can reduce the difference between the counters. This ensures that entries are aged out more frequently. It is important to note that the value of STCURR should never be left with the same value as STPURG.

Using the SDO_INCPR routine can be used for more than altering the data-aging rate. It can be used in severe conditions when the LANCAM database becomes full to remove older entries and increase the data-aging gap.

When this condition exists, the /INTR output is asserted by the MU9C8338 (if configured in STARG) to indicate an interrupt. The CPU must then read the System Status (SSTAT) register to confirm the cause of the interrupt. The SDO_INCPR can be invoked to remove some of the entries from the database. Initiating a single purge of older entries may not delete anything because there may be no entries in the database that have the same time stamp value as the one to be purged. Therefore, it is recommended that the purge routine is invoked repeatedly until an entry or entries have been deleted. The SSTAT register must be monitored after invoking the SDO_INCPR routine to check if the LANCAM /FF has returned to its normal status. Table 13 shows how the SDO_INCPR can be used to remove entries in this way. Lines 1 and 2 can be repeated until sufficient entries have been deleted from the database.

Increment/Purge Time Stamp Counter Routines

The third routine is the increment time stamp and purge time stamp counters routine and is triggered in two ways. It can be triggered by writing to the SDO_INCTSPR register or by asserting the INCR hardware input (if it is configured in the STARG register). This built-in routine is used for the normal purging or aging out of older entries. The routine increments both the STCURR and STPURG counters (shown in Table 14), keeping the data-aging gap constant, and deleting any matching LANCAM entries as described earlier. The CPU should perform this task at regular intervals to remove older entries from the database.

Table 11: Decreasing the Data-Aging Gap by Increasing the STCURR Value

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	26H	xxxxH	SDO_INCTS	Trigger the increment STCURR sequence	1

Notes:

1. xxxx = Don't care

Table 12: Increasing the Data-Aging Gap by Increasing the STPURG Value

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	26H	xxxxH	SDO_INCPR	Trigger the increment STPURG sequence	1

Notes:

1. xxxx = Don't care

Table 13: Purge Older Entries by Invoking the Increment STPURG Sequence

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	27H	xxxxH	SDO_INCPR	Trigger the increment STPURG sequence	1
2	L	H	00H	Status bits Bit 0 = /FF	SSTAT	Read the SSTAT register to identify condition of LANCAM Full flag	2

Notes:

1. xxxx = Don't care

2. The SSTAT register has the status of the LANCAM Full flag in bit [0]. If bit 0=0, the LANCAM is full and if bit 1=1, the LANCAM has at least one empty location. Bits [15:1] can be ignored during the register read.

Table 14: Purge Older Entries by Invoking the Increment STPURG and STCURR Sequence

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	28H	xxxxH	SDO_INCTSPR	Trigger the increment time stamp and purge sequence	1

Notes:

1. xxxx = Don't care

Notes

Notes

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