MUSIC SEMICONDUCTORS

Application Note AN-N29

IP Over ATM

INTRODUCTION

In order to transport IP (Internet Protocol) traffic over ATM (Asynchronous Transfer Mode) networks, the IP address needs to be translated to a VPI (Virtual Path Identifier) and VCI (Virtual Channel Identifier) pair. At the other end of the network, the VPI/VCI pair needs to be translated back to the IP address. As the port speeds increase, and the port densities of switching systems increase, the need for fast, deterministic translation becomes increasingly important. In addition, applications like VoIP or video are extremely sensitive to jitter, and systems are required to minimize or eliminate any transit time variation.

Using MUSIC Semiconductors devices as translation engines, the translation time is fixed, regardless of database depth. Using the MUSIC Semiconductors MU9C8K64–50TDC RCP (Routing Co-Processor), 28 ports of OC-3 could be supported for bidirectional mapping, and 54 ports for unidirectional mapping. This translation method works equally well for assigned VPI/VCI combinations, PVCs (Permanent Virtual Circuits), and SVCs (Switched Virtual Circuits). For simplicity and clarity, this document refers to assigned VPI/VCI pairs. Simple changes would support broader cases.

IP OVER ATM: BIDIRECTIONAL MAPPING

MUSIC Semiconductors Content Addressable Memories (CAMs) and Routing Co-Processors (RCPs) provide one-to-one mapping of IP addresses to ATM VPI/VCI addresses. The 64-bit wide MUSIC CAM word can be partitioned into two 32-bit wide segments at the same physical address.

One 32-bit segment is the CAM partition, or Associative Data field. The second 32-bit segment is the RAM partition, or Associated Data field. A search for the IP address in the CAM segment returns the associated VPI/VCI pair (and PTI bits, if used) in the RAM segment. The CAM/RAM partition could then be switched so the VPI/VCI pair could be searched for in the CAM partition. In this case, the RAM partition would return the corresponding IP address. In either case, additional associated data could be stored in external SRAM, indexed by the data address of the IP-VPI/VCI location. The routines at the end of this document include the optional READ instruction for the Search, Insert, and Delete routines.

The host processor is required to set up and tear down the ATM connection, and make the initial mapping decision. Once the IP address is mapped to a VPI/VCI pair, the system will switch the traffic at full wire speed, without host processor intervention. Inserting and deleting connections is quick and simple using CAMs and RCPs. Please refer to the latest device datasheets for detail information on the individual products.

INITIALIZATION AND CONFIGURATION

The Initialization routines at the end of this document set up the MUSIC devices to use 32 bits of the 64-bit word for the IP Address, and the remaining 32 bits for the VPI/VCI pair (and possibly the PTI bits). This allows either 32-bit field to be searched easily and quickly.

For the LANCAM, LANCAM 1st and WidePort LANCAM devices, the foreground register set is configured for IP to ATM VPI/VCI translation. The background register set is configured for ATM VPI/VCI to IP address translation.

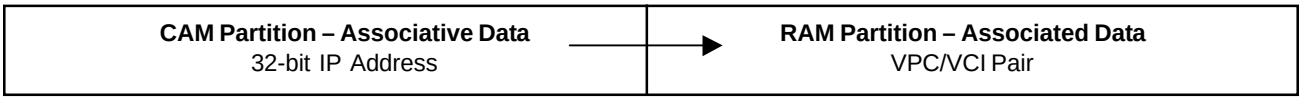

Figure 1: 64-bit Word – IP Address Search

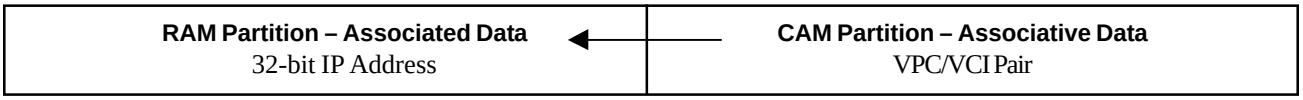

Figure 2: 64-bit Word – VPI/VCI Search

Deletion of entries is expected to be initiated on the ATM side, so the Delete Entry routine uses the background register set.

Using the MU9C RCP Family, the user has direct control over which 32-bit segment is being written to and read from. This allows the translation process to be more efficient, and simplifies the procedure for adding new entries.

SEARCHING THE TRANSLATION DATABASE

The map database is set up so that only one database entry is required per mapping regardless of which direction needs to be resolved. Either of the two main fields of the database can be searched, returning the value contained in the other field of the matching location.

A third field is the address of the matching location, which could be used to index into external RAM for additional associated data fields, if necessary.

Although the IP (Layer 3) Address is known, the switch needs to know the corresponding VPI/VCI pair in order to forward the packet. In this mode, the CAM or RCP is searched for the IP Address and returns the mapped VPI/VCI pair, and the index for external associated data, if used. Similarly, if the VPI/VCI pair is known, the corresponding IP Address is being sought. A search of the VP/VC table will return the mapped IP Address and the index for external associated data, if used. Either way, the MU9C RCP Family, for example, would perform the search and read operation in 120 ns, using a 15 ns master clock with the 50 ns speed grade device.

The Search Routines at the end of this document outline all of the steps necessary to perform searches for each of MUSICs 64-bit wide devices.

INSERTING A NEW ENTRY

When using CAMs and RCPs as search engines, it is not necessary to sort the entries. This will not improve performance of the search engine. This simple feature of CAMs and RCPs greatly simplifies the addition of new entries. Both the IP Address and the corresponding VPI/VCI are written to the device. The entry location may be read as an index so that an external RAM table could be used to store additional associated data. For the MU9C RCP Family, adding an entry would consume 120 ns, using a 15ns master clock with the 50 ns device.

DELETING AN ENTRY

Deleting an entry is handled from the ATM side, since call setup and teardown is easily handled in ATM. A search of the VPI/VCI pair will locate the entry in the CAM or RCP device. Reading the index will allows the removal of external associated data, if used. The final step is to mark the CAM or RCP location as "Empty," removing it from the active table.

DEVICE ROUTINES

LANCAM, LANCAM 1st

Initialization Routine

Cycle	Hex	Description
CRS	0x0000	Dummy Read cycle; Clears power-up anomalies
CWS	0x0200	TCO_CT; Target Control register
CWM	0x0000	0x0000; Reset
CWS	0x0228	TCO_DS (LANCAM only)
CWM	0xFFFF	Set DS=FFFF (LANCAM only)
CWS	0x0208	TCO_PA (LANCAM only)
CWM	0x0000	Set PA=0 (LANCAM only)
CWS	0x0228	TCO_DS (LANCAM only)
CWM	0x0000	Set DS=PA (LANCAM only)
CWS	0x0200	TCO_CT; Target Control register
CWM	0x0080	32 CAM, 32 RAM, Increment Address register
CWS	0x0210	TCO_SC; Target Segment Control register
CWM	0x0AC2	Write to Segments 0:1, Read Segments 2:3
CWS	0x0100	SPD_CR; Set Persistent Destination to Comparand register
CWS	0x0005	SPS M@HM; Set Persistent Source to Memory at Highest Match
CWS	0x0619	SBR
CWS	0x0200	TCO_CT; Target Control register
CWM	0x0140	32 RAM, 32 CAM, Increment Address register
CWS	0x0210	TCO_SC; Target Segment Control register
CWM	0x5850	Write to Segments 2:3, Read Segments 0:1
CWS	0x0100	SPD_CR; Set Persistent Destination to Comparand register
CWS	0x0005	SPS_HM; Set Persistent Source to Memory at Highest Match

Legend:

CWS: Command Write, Short Cycle
CRS: Command Read, Short Cycle
CWM: Command Write, Medium Cycle
CRM: Command Read, Medium Cycle
CWL: Command Write, Long Cycle
DWS: Data Write, Short Cycle
DWL: Data Write, Long Cycle
DRL: Data Read, Long Cycle
xxxx: Don't Care
aaa: Address
dddd: Data

Please refer to the individual device datasheets for the detail information.

DEVICE ROUTINES *Continued*

LANCAM, LANCAM 1st

Search IP Address Routine

Cycle	Hex	Description
CWS	0x0618	SFR; Set Foreground Register set
DWS	0xdddd	Write 1st 16 bits of IP Address
DWL	0xdddd	Write Last 16 bits of IP Address and Compare
DRL	0xdddd	Read 1st 16 bits of VPI/VCI
DRL	0xdddd	Read remaining bits of VPI/VCI
CRM	0x0aaa	Read CAM Address (Optional)

Search VPI/VCI Routine

Cycle	Hex	Description
CWS	0x0619	SBR; Set Background Register set
DWS	0xdddd	Write 1st 16 bits of VPI/VCI Address
DWL	0xdddd	Write Last 16 bits of VPI/VCI Address and compare
DRL	0xdddd	Read 1st 16 bits of IP Address
DRL	0xdddd	Read remaining 16 bits of IP Address
CRM	0x0aaa	Read CAM Address (Optional)

Insert Entry Routine

Cycle	Hex	Description
CWS	0x0618	Set Foreground Register set
CWS	0x0210	TCO_SC
CWM	0x1800	Write Segments 0:3
DWS	0xdddd	Write 1st 16 bits
DWS	0xdddd	Write 2nd 16 bits
DWS	0xdddd	Write 3rd 16 bits
DWS	0xdddd	Write 4th 16 bits of IP Address
CRM	0x0aaa	Read Next Free Address (Optional)
CWL	0x0334	MOV_NF CR, V- Move to Next Free, mark Valid
CWS	0x0210	TCO_SC
CWM	0x0AC2	Write to Segment 0:1, Read Segments 2:3

Delete Entry Routine

Cycle	Hex	Description
CWS	0x0619	SBR; Set Background Register set
DWS	0xdddd	Write 1st 16 bits of VPI/VCI Address
DWL	0xdddd	Write Last 16 bits of VPI/VCI Address and Compare
CRM	0x0aaa	Read CAM Address (Optional)
CWM	0x042D	VBC_HM, E - Mark Highest Matching location Empty

Legend:

CWS: Command Write, Short Cycle
CRS: Command Read, Short Cycle
CWM: Command Write, Medium Cycle
CRM: Command Read, Medium Cycle
CWL: Command Write, Long Cycle
DWS: Data Write, Short Cycle
DWL: Data Write, Long Cycle
DRL: Data Read, Long Cycle
xxxx: Don't Care
aaa: Address
dddd: Data

Please refer to the individual device datasheets for the detail information.

DEVICE ROUTINES *Continued*

WIDEPORT LANCAM

Initialization Routine

Cycle	Hex	Description
CRS	0x0000 0000	Dummy Read Cycle; Clears power-up anomalies
CWM	0x0200 0000	TCO_CT; Target Control Register and Reset
CWM	0x0228 FFFF	TCO_DS; Set DS=FFFF
CWM	0x0208 0000	TCO_PA; Set PA=0
CWM	0x0228 0000	TCO_DS; Set DS=PA
CWM	0x0200 0080	TCO_CT; 32 CAM, 32 RAM, Increment Address register
CWM	0x0210 0141	TCO_SC; Write to Segment 0, Read Segment 1
CWS	0x0100 0000	SPD_CR; Set Persistent Destination to Comparand register
CWS	0x0005 0000	SPS M@HM; Set Persistent Source to Memory at Highest Match
CWS	0x0619 0000	SBR
CWM	0x0200 0140	TCO_CT; 32 CAM, 32 RAM, Increment Address register
CWM	0x0210 2808	TCO_SC; Write to Segment 1, Read Segment 0
CWS	0x0100 0000	SPD_CR; Set Persistent Destination to Comparand register
CWS	0x0005 0000	SPS M@HM; Set Persistent Source to Memory at Highest Match

Search IP Address Routine

Cycle	Hex	Description
CWS	0x0618 0000	SFR; Set Foreground Register set
DWL	0xdddd dddd	Write IP Address and Compare
DRL	0xdddd dddd	Read VPI/ VCI
CRM	0xXXXX 0aaa	Read CAM Address (Optional)

Legend:

CWS: Command Write, Short Cycle
CRS: Command Read, Short Cycle
CWM: Command Write, Medium Cycle
CRM: Command Read, Medium Cycle
CWL: Command Write, Long Cycle
DWS: Data Write, Short Cycle
DWL: Data Write, Long Cycle
DRL: Data Read, Long Cycle
xxxx: Don't Care
aaa: Address
dddd: Data

Please refer to the individual device datasheets for the detail information.

DEVICE ROUTINES *Continued*

WIDEPORT LANCAM

Search VPI/ VCI Routine

Cycle	Hex	Description
CWS	0x0619 0000	SBR; Set Background Register set
DWL	0xdddd dddd	Write VPI/ VCI Address and Compare
DRL	0xdddd dddd	Read IP Address
CRM	0xXXXX 0aaa	Read CAM Address (Optional)

Insert Entry Routine

Cycle	Hex	Description
CWS	0x0618 0000	Set Foreground Register set
CWM	0x0210 0C04	TCO_SC; Write Segment 0:1
DWS	0xdddd dddd	Write IP Address
DWS	0xdddd dddd	Write VPI/ VCI
CRM	0xXXXX 0aaa	Read Next Free Address (Optional)
CWL	0x0334 0000	MOV_NF CR, V- Move to Next Free, mark Valid
CWS	0x0210 0141	TCO_SC; Write Segment 0, Read Segment 1

Delete Entry Routine

Cycle	Hex	Description
CWS	0x0619 0000	SBR; Set Background Register set
DWL	0xdddd dddd	Write VPI/ VCI Address and Compare
CRM	0xdddd 0aaa	Read CAM Address (Optional)
CWM	0x042D 0000	VBC_HM, E - Mark Highest Matching location Empty

Legend:

CWS: Command Write, Short Cycle
CRS: Command Read, Short Cycle
CWM: Command Write, Medium Cycle
CRM: Command Read, Medium Cycle
CWL: Command Write, Long Cycle
DWS: Data Write, Short Cycle
DWL: Data Write, Long Cycle
DRL: Data Read, Long Cycle
xxxx: Don't Care
aaa: Address
dddd: Data

Please refer to the individual device datasheets for the detail information.

DEVICE ROUTINES *Continued*

MU9C RCP

Intialization Routine

Cycle	AC Bus	/AV	DQ Bus	Description
		1	0xXXXX X006	Load Instruction register
		0	0x0200 0000	Execute, Set to Hardware Mode
WR DS	XXX 000 001 000	1	0xXXXX X100	Disable Device Select register
WRH MR1	XXX 001 001 001	1	0x0000 0000	Mask Register if IP Address Search
WRL MR1	XXX 001 001 001	1	0xFFFF FFFF	Mask Register if IP Address Search
WRH MR2	XXX 010 001 001	1	0xFFFF FFFF	Mask Register for VPI/ VCI Search
WRL MR2	XXX 010 001 001	1	0x0000 0000	Mask Register for VPI/ VCI Search

Search IP Routine

Cycle	AC Bus	/AV	DQ Bus	Description
CMPWL DQ	XXX 001 011 010	1	0xdddd dddd	Write IP Address and Compare
RDH [HPM]	XXX XXX 000 010	1	0xdddd dddd	Read VPI/ VCI

Search VPI/ VCI Routine

Cycle	AC Bus	/AV	DQ Bus	Description
CMPWH DQ	XXX 010 011 010	1	0xdddd dddd	Write VCI/ VCI and Compare
RDL [HPM]	XXX XXX 000 010	1	0xdddd dddd	Read IP Address

Insert Entry Routine

Cycle	AC Bus	/AV	DQ Bus	Description
WRL [NFA]	XXX 000 000 001	1	0xdddd dddd	Write IP Address
WRH [NFA]	XXX 000 000 001	1	0xdddd dddd	Write VPI/ VCI

Delete Entry Routine

Cycle	AC Bus	/AV	DQ Bus	Description
CMPWH DQ	XXX 010 011 010	1	0xdddd dddd	Write VPI/ VCI and Compare
WRH [NFA]	XXX XXX 100 001	1		Reset Validity Bit (Delete Entry)

Legend:

WR: Write
WRH: Write Higher 32 Bits
WRL: Write Lower 32 Bits
RDH: Read Higher 32 Bits
RDL: Read Lower 32 Bits
CMPWH DQ: Write Higher 32 Bits & Compare
CMPWL DQ: Write Lower 32 Bits & Compare
DS: Device Select Register
MR1: Mask Register 1
MR2: Mask Register 2
HPM: Highest Priority Match
NFA: Next Free Address
RST V@[HPM]: Reset Validity bit at Highest Priority Match
XXXX: Don't Care
dddd: Data

Please refer to the individual device datasheets for the detail information.

NOTES

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