Using the MU9C8358L 10/100Mb Ethernet Filter Interface in Switch Applications

INTRODUCTION

The MUSIC MU9C8358L is a quad 10/100Mb Ethernet filter interface ideal for switch applications. The MU9C8358L provides the user with a high performance, large capacity Ethernet address processing subsystem when used in conjunction with the MUSIC MU9Cx480B LANCAM family. It also has internal arbitration logic that allows two devices to be connected together to support up to eight 10/100Mb Ethernet ports at wire speed. When connected in this way, both devices share the same LANCAM database, simplifying the design while offering a cost efficient solution.

In a typical switch application, the MU9C8358L parses incoming frames for both the source address (SA) and the destination address (DA). It then automatically performs all the address table lookup functions required to allow the switch routing control hardware to make the correct forwarding decision. Time stamps are added or updated automatically during the address table lookups, which removes the need for additional management software. A group of built-in routines enables the system to purge older entries from the database, adjust the time stamps, and add and remove permanent entries when required.

This Application Note describes how the MU9C8358L can be used to accelerate packet switching. The functionality of the device is described in detail with emphasis given to the input and output signals required when transferring data. Software and hardware examples are provided to show how two MU9C8358L devices would be configured and used in a typical 8-port 10/100Mb switch. Figure 1 shows the block diagram of a typical switch incorporating two MU9C8358L devices and a LANCAM database.

FUNCTIONAL DESCRIPTION

The MU9C8358L is used in switch applications to extract and process the address information from incoming packets. After parsing the DA and SA, the MU9C8358L provides the appropriate information so that the packet is switched to the correct outgoing port. In order to make this decision, the MU9C8358L compares the DA with a table of addresses stored in an external CAM memory.

After the comparison is performed, the result is available to the surrounding hardware through a result output port or by reading an internal software register. If the comparison yields a match, then the port identification is given so that the routing control hardware may forward the packet to the correct port. If the DA is not found in the address table, the packet is forwarded to all the ports in the switch, except for the port that received it.

The MU9C8358L will also compare the SA of the received packet. If it is not found, then it is added to the table along with the identification of the port to which it belongs. However, if a match is found, the port number is updated in order to keep the address database accurate. An 8-bit time stamp value is also automatically added to the table entries as they are added or updated. This allows the switch to delete older entries at regular intervals in order to remove address information that is no longer valid. The host CPU has full control over the time stamping mechanism to adjust the time that entries stay in the database. This allows the life of an entry to be increased when network traffic is low and decreased when network traffic is high. The routine that purges entries can be invoked by asserting a hardware pin or by writing to a software register.

Typically, in a switch such as the one shown in Figure 1, two MU9C8358Ls and their associated LANCAMs would be initialized and configured by the host CPU to perform all the DA and SA filter operations automatically as each packet is received. As each packet is processed, the MU9C8358L indicates that the result is available by asserting a result port hardware pin. An optional interrupt also can be sent to the host processor if required. The result is read by external hardware through a result port or by the CPU by checking an internal register. This result is interpreted by the routing control hardware, which switches the packets appropriately. The MU9C8358L also has other built-in routines that allow simple management tasks to be performed. The routines that are included allow permanent entries to be added/removed, allow entries to be read out, and allow older entries to be purged. The host CPU selects the routines by writing to the appropriate 16-bit System Command register. A full description of how to configure the MU9C8358L and to operate the additional routines is given later in the Application Note.

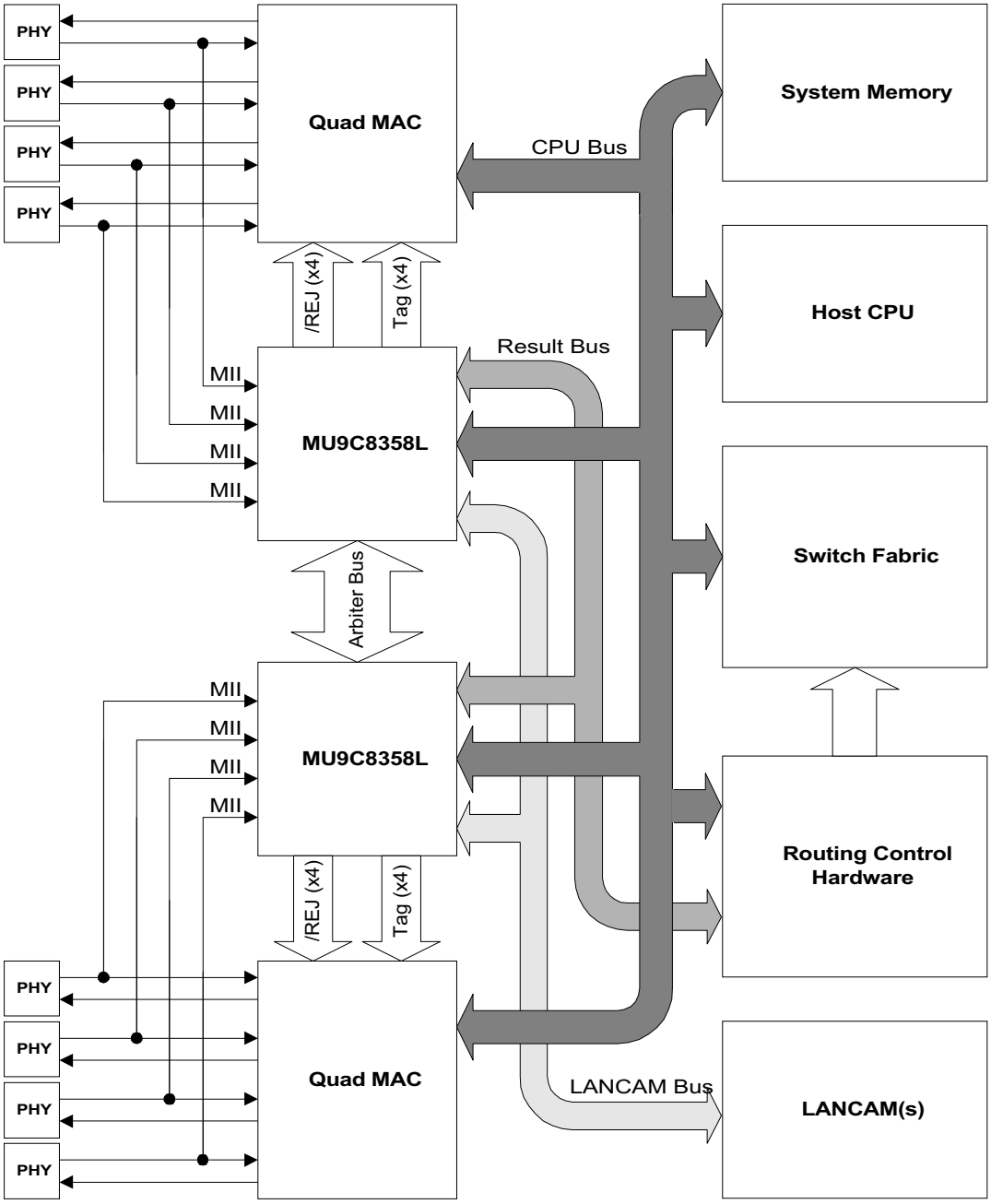

Figure 1: 8-Port Switch Example

HARDWARE IMPLEMENTATION

The MU9C8358L has six distinct interface ports that are used when transferring data to and from the device. They are the Processor port, Result port, LANCAM Interface, Arbiter, JTAG Test Access port, and the set of four IEEE 802.3 Standard Media Independent Interface (MII) and Tag ports. These can be seen in the system block diagram in Figure 2. This section explains how each interface port should be configured when two devices are used together to support eight 10/100Mb ports.

Processor Port

The Processor port is used to transfer data to and from the MU9C8358L's three internal register sets. This allows the host CPU to initialize and configure both the internal registers and the LANCAM database and perform general system management and maintenance tasks. When configuring the LANCAM(s) for use in a typical switch, they are not accessed directly by the host processor. Instead, writing commands to the LANCAM Control Signals (SLCCS) and CAM Data Word 0 (SCDW0) register allows the LANCAM(s) to be properly configured. Once the configuration has been completed, the general system tasks also are performed through the Processor port by writing to the appropriate System Command register. The tasks include initiating the deletion of older entries from the LANCAM database and other general management duties.

The Processor port consists of a 16-bit data bus (D[15:0]), 8-bit address bus (A[7:0]) and the associated signals required for successful data transfer. The MU9C8358L has three sets of internal registers that are accessed by loading the appropriate address on A[7:0] while asserting the required chip select. /PCSS is the Processor Chip Select System and must be asserted LOW to access the 23 System registers. Both devices would share /PCSS if two MU9C8358Ls are connected together. However, /PCS is the Processor Chip Select and must be individually asserted LOW to access the four Chip registers and the 16 Port registers in each device. It is recommended that some form of memory mapping and address decoding scheme is used in order to gain access to the required registers. Therefore, if two MU9C8358Ls are used together, three base address values are required. One for the combined /PCSS signal, and one for each of the individual /PCS signals. Figure 3 shows the connections to both Processor ports when two devices are cascaded.

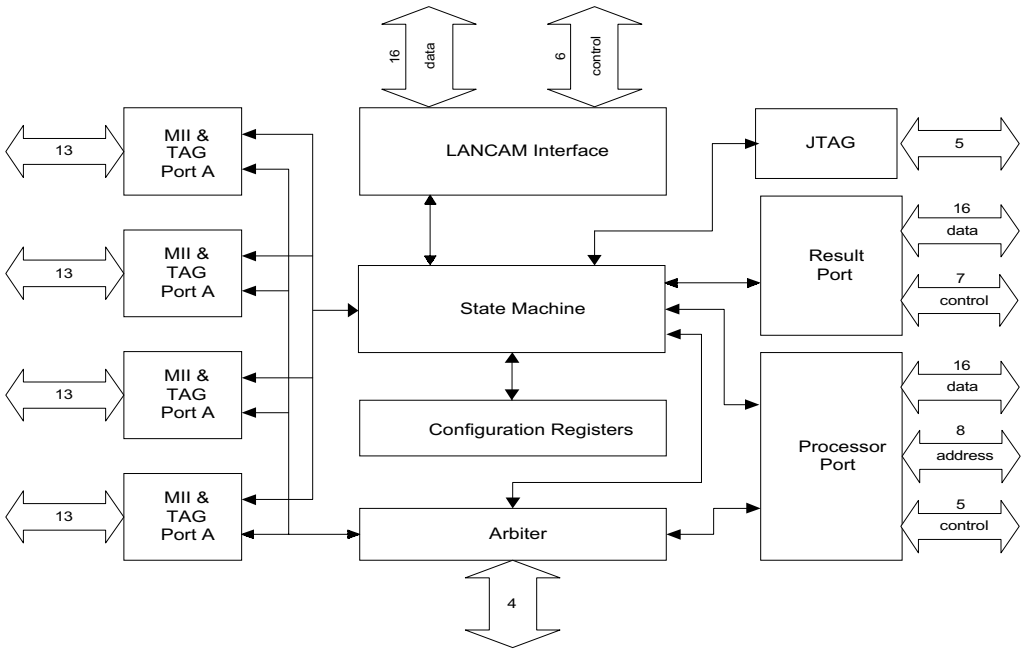

Figure 2: MU9C8358L System Block Diagram

The /WRITE input determines the direction of data flow into or out of the processor port. If it is LOW, the data placed on D[15:0] is written to the specified register. On the other hand, if it is HIGH, the contents of the required register is placed on D[15:0] by the device. PROC_RDY is a tri-state output from the MU9C8358L that ensures successful data transfer. When reading from or writing to the internal registers, the MU9C8358L asserts PROC_RDY to indicate that the data was received or the data was placed on the bus. When two devices are used, both PROC_RDY outputs should be connected together. When it is the System registers that are being written to or read from, only the device configured as the master will drive its output. The Port and Chip registers are individual to each device ensuring only one device is driving the output at any one time.

The /INTR output is used to indicate an interrupt to the host CPU. The user configures whether certain events will cause an interrupt by setting the appropriate bits in the System and Port Target registers. The possible causes of an interrupt that can be configured are:

- The MU9C8358L has processed a packet's DA and the result is available. The Result Status (RSTAT) register must be read to determine if there is result data available. The data can be read by accessing the Result Data (RDAT) register. A subsequent read of the RDAT register will return the next result. When one result has been read, any interrupt service routine should read RSTAT again to confirm if there is any further data to be read. The /INTR pin will return to its normal state when all the result data has been read. Alternatively, the result data can be accessed directly through the hardware result port. If this port is used to access the data, it is recommended that the result interrupt not be configured. Instead the RP_DV output should be monitored by external hardware to detect when result data is available.
- The LANCAM is full. The /INTR pin is returned to its normal state when the System Status (SSTAT) register is read and an entry has been removed from the LANCAM. The built-in routine can be invoked until the LANCAM FULL condition is no longer true.

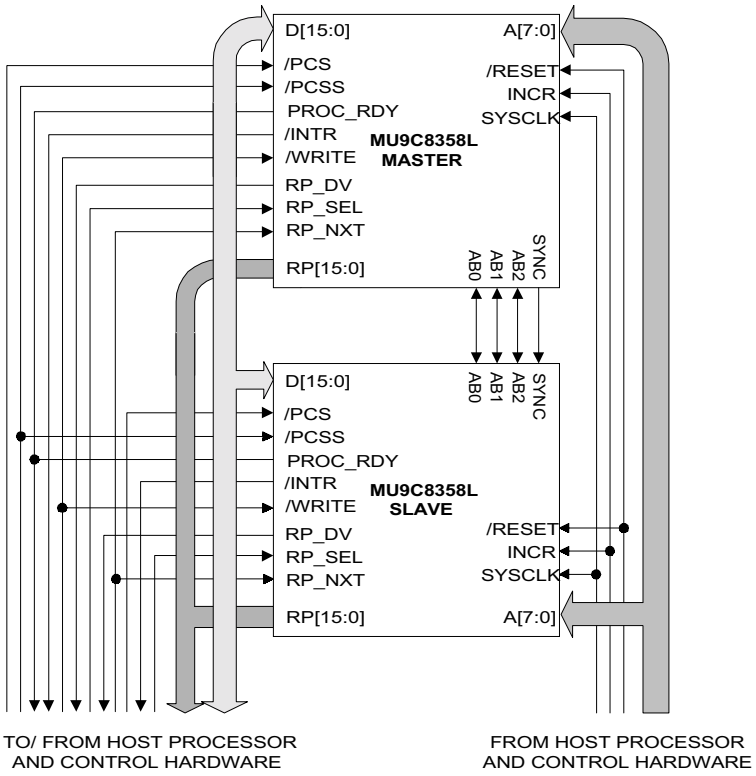

Figure 3: Two MUC9C8358Ls Cascaded Together

When two devices are used, the individual /INTR outputs should be monitored to detect which device has signaled an interrupt. An interrupt service routine should respond to an interrupt by checking each register in turn until the cause has been found. For a detailed description of each signal and for the required timing specifications, please refer to the MU9C8358L data sheet.

Result Port

After the MU9C8358L has been configured correctly, it parses incoming frames to extract the DA and SA. It automatically performs the required LANCAM database processing functions so that the switch hardware can forward the packet to the correct port(s). The Result Port is the 19-bit interface that allows the MU9C8358L to communicate the DA search results. RP[15:0] is the 16-bit output that transfers the result data to the surrounding switch hardware. The result information that is available after each incoming packet has been parsed and analyzed is shown in Table 1. This data is also available to the host CPU by reading the internal RDAT register. The bit mapping of the RDAT register is identical to the data that is available through the result port.

It is important to note that although the result data is available through the Result Port and the Processor Port, the source is mutually exclusive. Therefore, any data read from the Result Port is not also transferred to the RDAT register. In the same way, if the user uses the RDAT register to access the data, the Result Port should not be used to ensure all data reaches the register.

From the result information, the incoming packets can be rejected or forwarded to the appropriate outgoing port(s). Three control signals are required to read the results as each incoming packet is processed. The MU9C8358L indicates that there is result data by asserting RP_DV HIGH. The RP_NXT, and RP_SEL inputs are used to transfer the data to the surrounding hardware.

RP_DV remains HIGH while there is valid result data available at the 16-bit RP[15:0] output. RP_NXT and RP_SEL control the transfer of the valid data to the interface hardware. RP_SEL is the result port tri-state control and loads the RP[15:0] with the data when it is asserted HIGH. If two devices are connected together as in Figure 3, the device that has valid data is selected by asserting its RP_SEL input. If only one device is used, this input can be held HIGH if required.

RP_NXT is asserted HIGH to clock out the next result from RP[15:0] (RP_SEL must also be HIGH). If there is further result data to be read, RP_DV will continue to remain HIGH 140ns after RP_NXT is asserted. If there is no further data, RP_DV will go LOW 140ns after RP_NXT is asserted. When the RDAT register is read through the Processor Port in order to read results, RP_SEL and RP_NXT should remain LOW. This ensures that all the valid data reaches the register. If two devices are cascaded, the RP_NXT inputs should be connected together. Only the device that has been selected by asserting RP_SEL HIGH will respond to the RP_NXT input. For a detailed description of each signal and for the required timing specifications, please refer to the MU9C8358L Data Sheet.

Table 1: Result Port Bit Descriptions

Bit(s)	Description
15:10	Source Port ID: These bits indicate which of the four MII ports the packet was received through.
9:8	Packet Type: This indicates if the packet that was processed was a broadcast (00), multicast (01), or unicast (10) packet.
7	Match Found: If the processed packet was unicast, this bit indicates whether a match was found during the destination address lookup. This bit is logic 1 for a match and logic 0 for no match.
6:1	Destination Port ID: If there was a match found (bit 7 = 1), these bits indicate to which of the four MII ports the external switch hardware should forward the packet.
0	Destination Port = Source Port: This bit indicates (if a DA match was found) that the source of the packet was the same as the destination of the packet. Therefore there is no need to forward this packet to any other MII port.

LANCAM Interface

The LANCAM interface consists of the signals DQ[15:0], /E, /W, /CM, /EC, /RESET_LC, /MI, and /FI. These are connected directly to the MU9Cx480B LANCAM devices that are used to store the address database. When the MU9C8358L has to perform any operations on the LANCAMs it will load these outputs with the appropriate signal values. LANCAMs can be cascaded to increase the depth of the address table. The timing of the LANCAM interface is such that it will accommodate up to four LANCAMs cascaded as in Figure 4.

If fewer than four LANCAMs are required, Figure 4 is amended by removing the lowest-priority device(s) (CAM 0 is the highest-priority device) and the inputs that are connected to it. Connect the /FF and /MF outputs from the new lowest-priority device to the /FI and /MI inputs of both MU9C8358Ls. If the depth of the system address table requires more than four LANCAMs to be cascaded, an external prioritization method can be used. However, when using this method, care must be taken to ensure that the flag-ripple timing requirements are satisfied. The appropriate LANCAM data sheet gives a full description of how LANCAMs can be cascaded using each method.

The MU9C8358L will load /E, /W, /CM, /EC, and DQ[15:0] with the appropriate signal values to perform all the necessary LANCAM operations. The /FI and /MI inputs indicate the match and full status of the database and are connected to only the last LANCAM's /FF and /MF outputs. /RESET_LC is the reset output from the MU9C8358L and is used to reset the LANCAMs. It is connected to only the master device when two are connected together. This output is asserted LOW when the system reset input (/RESET) is also asserted LOW. However, it will remain LOW after /RESET has been taken HIGH. Bit 0 of the System Dynamic Configuration register (SDCFG) must be set to logic 1 to return /RESET_LC HIGH and therefore allow normal operation of the LANCAMs.

Arbiter

Two MU9C8358L devices can be connected together by means of the Arbiter port. This allows up to eight 10/100Mb Ethernet ports to share the same LANCAM database. Once two devices are cascaded in this way, one becomes the master while the other becomes the slave. The Arbiter port consists of SYNC and ARB[2:0]. Once connected as master and slave, the master device must have its CHIPROL register loaded with 000b at initialization (see section on system configuration). Figure 3 on page 4 shows how the Arbiter port is connected when two devices are used. If only one MU9C8358L is used, the SYNC and ARB[2:0] pins may be left unconnected.

MII and Tag Ports

The MU9C8358L has four independent IEEE 802.3 Standard 10/100Mb MII ports that are used to receive incoming packets and parse them for address information. Typically the MII bus is "tapped" to collect packet data as it is passed from the switch port PHY to the MAC. Once the MII port receives the data, the MU9C8358L automatically extracts the source and destination addresses, performs the appropriate LANCAM lookups, and outputs the result.

The MU9C8358L also provides four Tag ports that communicate the destination port ID once the LANCAM lookups have been completed. This allows MAC devices that support Tag switching to attach the destination port ID to the packet before it is routed through the switch fabric. The Tag port also indicates if incoming packets should be rejected if the destination port ID was identical to the source port ID. If Tag switching is not supported or implemented, these outputs may be left unconnected.

JTAG Test Access Port

The MU9C8358L has an IEEE 1149.1 compliant JTAG Boundary Scan test access port interface. A serial input bit stream is applied to the TMS input to select the specific boundary scan test. Table 2 shows the test modes that are possible when using the Test Access port. The test data is applied to the internal architecture through the TDI input. The TDO output provides the output path for the test data. TCK is the test clock input and can operate at a frequency up to 10MHz. When the test mode is not being used this input should be tied to a valid logic level. Finally, the /TRST input is the reset input for the test access port. This normally should be connected to the /RESET input or must be held at a LOW logic level when the JTAG port is not being used. /TRST, TMS, and TDI have an internal pull up resistor (25K minimum). Please refer to the IEEE 1149.1 Standard for more information on using the JTAG functions.

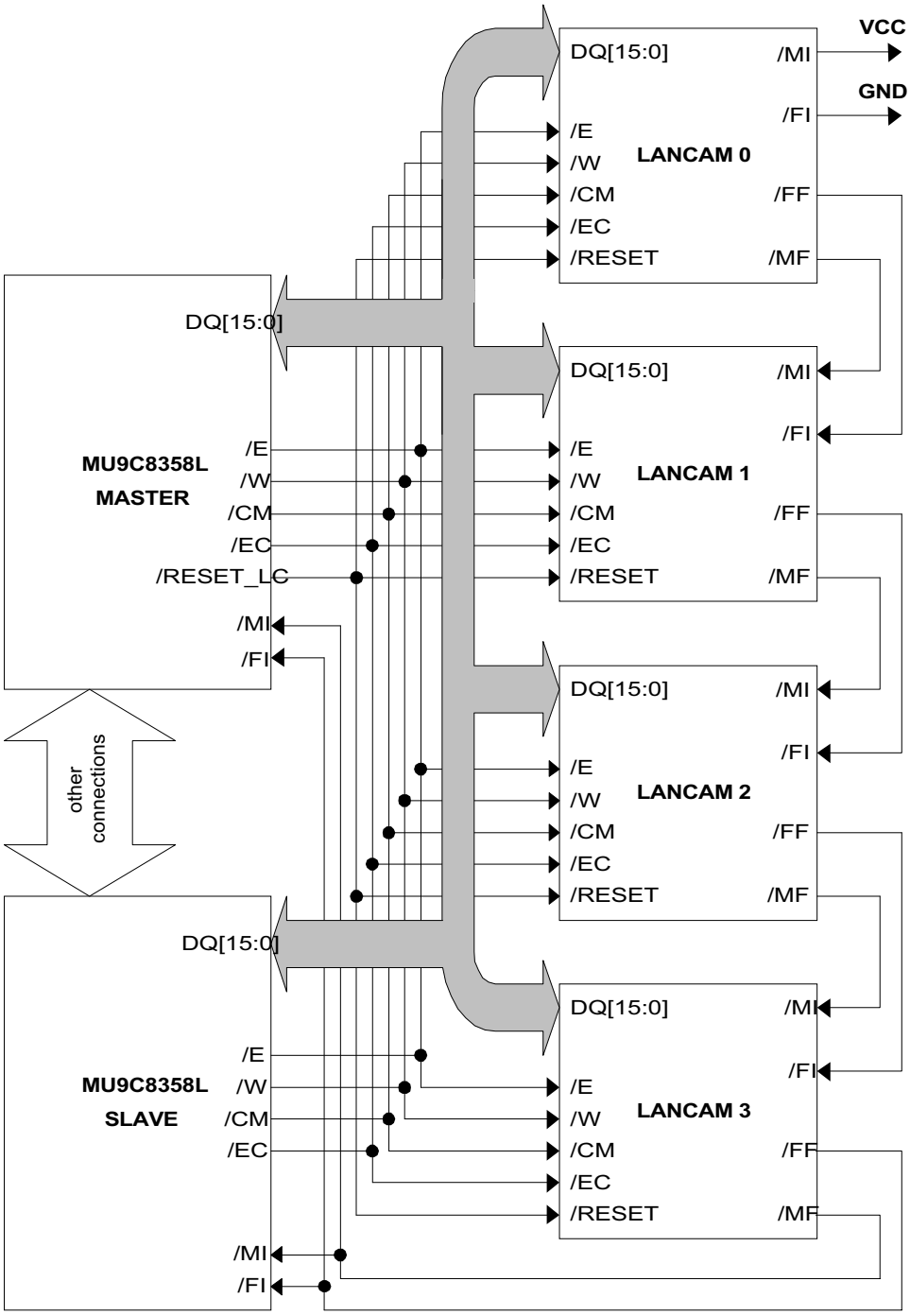

Figure 4: LANCAM Interface

Other Control Pins

The remaining control pins in the MU9C8358L are /RESET, INCR, and SYSCLK. /RESET is the main system reset input. This should be asserted LOW to perform a hardware reset. Before system initialization and configuration is begun to program the necessary registers, /RESET must be asserted LOW as shown in the System Configuration section.

The INCR input is the hardware purge control and is asserted HIGH. If this pin is enabled in the System Target register, asserting causes the following to happen:

1. Both the STCURR and STPURG registers are incremented. The new value of STCURR will be the 8-bit time stamp value that is added to LANCAM entries between this present time and the next INCR assertion.
2. The time stamps of each entry in the LANCAM database are compared with the new value of STPURG. All matching nonpermanent entries are deleted.

Typically, this pin would be asserted periodically to remove the older entries from the database to ensure the accuracy of the port ID information. Writing to the SDO_INCTSPR register also can perform this operation. This is explained in more detail in the General LANCAM Housekeeping section on page 20.

The SYSCLK input is the main system clock input and its frequency must be 50MHz.

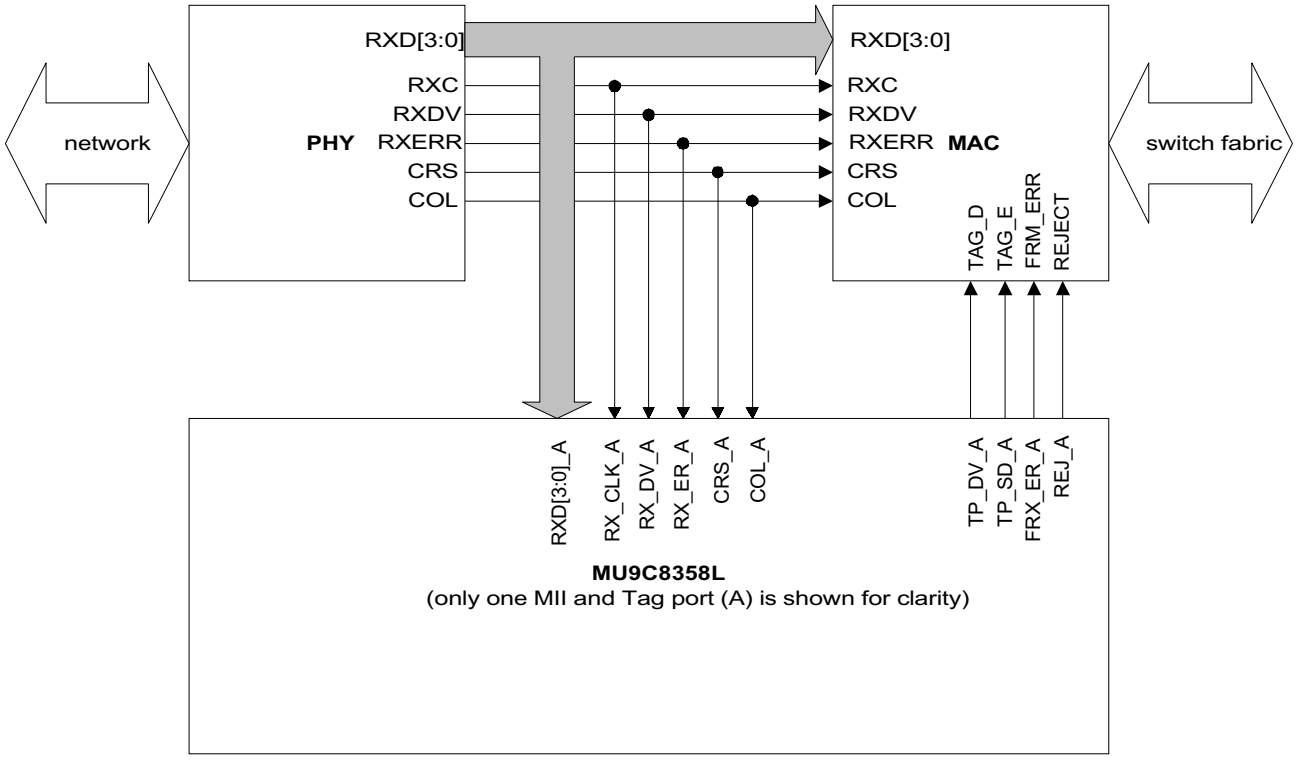

Figure 5: Connections for One MII and Tag Port

SOFTWARE INITIALIZATION AND CONFIGURATION

The MU9C8358L is designed to provide the user with a high performance, large capacity Ethernet processing subsystem. MUSIC MU9Cx480B LANCAM Family devices must be used to store the address table (MAC addresses and associated Port IDs). Once configured, the MU9C8358L will perform all the operations required to provide the surrounding switch hardware with the necessary forwarding information. The MU9C8358L also contains a number of built-in routines that allow the user to manually perform certain table management tasks. A group of System Command registers are used to invoke the appropriate routines once the appropriate information has been loaded into the CAM Data registers. These are explained in detail in the General LANCAM Housekeeping section on page 19.

This section will explain how LANCAMs are typically configured when they are used in switch applications. It will also explain how the LANCAMs are configured using a MU9C8358L System register to control the LANCAM interface port. Finally, it will show the steps that are required to initialize and configure the MU9C8358L registers and configure the LANCAMs that are used as the address database.

Table 2: JTAG Codes

Function	Code
EXT TEST	0000
BYPASS	1111
SAMPLE	0001
ID CODE	0010
CLAMP	0100
HIGH-Z	0011
INTEST	0101

LANCAM Configuration

The first operation that must be performed before the system will operate properly is configuration. The MU9C8358Ls and the LANCAMs must both be configured to perform all the functions required in a multi-port switch. The initialization and configuration of the LANCAM(s) involves setting the internal control registers with the operating conditions required in a multi-port layer 2 switch. For example, the control registers are set to allow the LANCAM(s) to store 48-bit MAC addresses and also return useful associated data in the remaining 16-bit segment.

The MUSIC LANCAM family has two sets of control registers that are known as the Foreground and Background Register sets. The Foreground registers are used when performing normal switch functions such as SA and DA lookups. The Background registers are used when performing the address table management tasks such as purging of older entries, setting the Address register and reading out entries. Table 3 shows how four LANCAM devices would be configured in a typical layer 2 switch.

Normally, individual commands are given to any LANCAM device by loading the signal inputs (DQ[15:0], /E, /CM, /EC, /W) with the appropriate values. The /E input to the LANCAM is the main enable input. It is asserted LOW to register the data and other control signals and returned HIGH to complete the cycle. Because the LANCAMs are connected directly to the MU9C8358L using the LANCAM interface, all these signal values are supplied by the MU9C8358L.

To allow the user to configure the LANCAMs, direct access is gained by setting bit 4 of the 16-bit System LANCAM Control Signals (SLCCS) register to logic level 1 while setting the other bits to the appropriate values. When using MUSIC LANCAMs, instructions are given or data is written to the device using the DQ[15:0] input/output pins. The control signals (/E, /CM, /EC, /W) are used to complete the data transfer cycle. Four cycles are possible: data write, data read, command write, and command read. The timing specifications that are required and a full description of all LANCAM functions can be found in the appropriate LANCAM Family data sheet.

The user should access the LANCAMs using the SLCCS register only during configuration. Once configuration is complete, Bit 4 of the SLCCS register should be set to logic level 0. There is no need to attempt to access the LANCAM after configuration using this register. Built-in routines have been included that will allow general LANCAM housekeeping operations to be performed. These are explained in the General LANCAM Housekeeping section, on page 19. When the user has control of the LANCAMs to read or write, the control outputs are manipulated by writing values to the SLCCS register.

Table 4 shows the register bit assignments that are required for each cycle used during configuration. Please note that a command read cycle is required only during initialization and configuration to clear up any power-up anomalies in the LANCAMs. To complete a LANCAM cycle during configuration, four distinct chronological steps must be followed to transfer data successfully to the LANCAMs. Table 5 shows the four steps that are required for each cycle. When performing the command read cycle that is required to clear power-up anomalies, step 1 is omitted.

Table 3: Typical Application Foreground and Register Settings

Register	Register Set	Description
Page Address	Shared	The Page address register of each device is set as follows: 1st device PA = 0, 2nd device PA=1, 3rd device PA=2, 4th device PA= 3. ***Note:*** *Only the first device PA is defined in a single LANCAM application.*
Control	Foreground	Set for 48 bits CAM, 16 bits RAM, the compares do not use a Mask Register, Enhanced Mode, the Address register increments.
Segment Control	Foreground	Set for writes to segments 3:0 and reads from segment 0 only.
Mask 1	Foreground	Segment 3=0000h, Segment 2=0000h, Segment1=0000h, segment 0=8000h. This is to mask the permanent bit in order to update only the PortID and time stamp during the automatic SA filter routine.
Persistent Destination	Foreground	This is set as Comparand Register.
Persistent Source	Foreground	This is set as Highest Match.
Control	Background	Set for 64 bits CAM, 0 bits RAM, the compares use Mask Register1, Enhanced Mode, the Address register increments.
Segment Control	Background	Set for writes to segment 0 only and reads from segment 3:0.
Mask 1	Background	Segment 3 = FFFFh, segment 2 = FFFFh, segment 1 = FFFFh, segment 0 = 7F00h.This is to mask the PortID in order to perform the purge routine.
Persistent Destination	Background	This is set as the Comparand Register.
Persistent Source	Background	This is set as the memory location that is specified by the Address Register.

Table 4: SLCC Register Individual Bit Assignments

Bit 4 CAM Access	Bit 3 /E	Bit 2 /W	Bit 1 /CM	Bit 0 /EC	16-bit SLCCS	Cycle
0	1	1	1	1	0Fh	The user has no direct access to the LANCAMs
1	1	0	0	1	19h	Command write with daisy chain locked (/E high)
1	0	0	0	1	11h	Command write with daisy chain locked (/E low)
1	1	1	0	1	1Dh	Command read with daisy chain locked (/E high)
1	0	1	0	1	15h	Command read with daisy chain locked (/E low)
1	1	0	1	1	1Bh	Data write with daisy chain locked (/E high)
1	0	0	1	1	13h	Data write with daisy chain locked (/E low)

Table 5: LANCAM Configuration Cycle Steps

Step	Register	Description
1	SCDW0	Write the Op-Code (command cycle) or the data to be transferred (data cycle) to the System CAM Data Word 0 (SCDW0) register. The MU9C8358L will load the DQ[15:0] pins of the LANCAM interface with the contents of this register during the cycle.
2	SLCCS	Write the appropriate value from Table 4 to the SLCCS register that will set up the LANCAM interface control outputs. This is the value that has /E set HIGH (e.g., 19h if it is a command write cycle).
3	SLCCS	Write the appropriate value from Table 4 to the SLCCS register that will begin the data transfer by asserting /E LOW (e.g., 11h if it is a command write cycle).
4	SLCCS	Write the appropriate value from Table 4 to the SLCCS register that will complete the data transfer by returning /E HIGH (e.g., 19h if it is a command write cycle).

System Configuration

After power-up or hardware reset, the host processor must perform the system initialization and configuration sequence. This involves setting the MU9C8358L System, Chip and Port registers to the values that are required for an 8-port 10/100Mb switch. Four MUSIC LANCAMs also are initialized and configured as described in the LANCAM Configuration section. The following reset sequence must take place in the order specified before the host processor performs the configuration sequence:

1. While /RESET is HIGH, RP_NXT must be held HIGH.
2. While /RESET is HIGH, RP_SEL must be held LOW.
3. While /RESET is HIGH, INCR must be held LOW.
4. /RESET is asserted LOW for a minimum of 1 ms and then returned HIGH.
5. RP_NXT, RP_SEL, and INCR may be set to any appropriate valid level.

Table 6 on page 14 shows the configuration sequence in full. The host CPU will write the values shown to the appropriate registers. A memory-mapping scheme should be used to decode the relevant chip select signal to the MU9C8358L. /PCS is asserted, after address decoding, when the individual Port or Chip registers are the targets. When two MU9C8358Ls are connected together, as described in this note, each device should have its own decoded /PCS signal. /PCSS is asserted, after address decoding, when the System registers are the targets. The configuration sequence is described as follows:

Line 1 selects the device that has been hardware configured as the MASTER device and sets its CHIPROL register to be 00H (master device). Line 2 sets the System Static Configuration register for 70ns LANCAMs and sets the port REJ output to be active LOW. Line 3 sets the System DA/SA Cycle register to accommodate the 70ns LANCAMs selected in line 2. Line 4 sets the System Dynamic Configuration register to enable the LANCAM devices. This will take the /RESET_LC output in the LANCAM interface HIGH and therefore allow the LANCAMs to function normally.

Lines 5 through 8 set the Port IDs in the MASTER device and lines 9 through 12 sets the Port IDs in the SLAVE device. It is important to note that the four Port Configuration (PCFG) registers have a default setting of 00H, which disables the 10 Base-X CRC facility. The configuration in this application note does not require the CRC facility and therefore the PCFG registers are left with their default settings. If this facility is to be enabled in the users specific application, it is recommended that it be performed between lines 12 and 13.

Lines 13 through 186 initialize and configure the four LANCAMs to operate properly with the built-in LANCAM system routines. Lines 13 and 14 set the System LANCAM Control Signals register to 0FH for two cycles. This is to ensure that the LANCAM interface outputs are in a safe mode before direct access to the LANCAM is enabled. Line 15 presets the LANCAM interface to the values required for a command read cycle before direct access is selected. The subsequent LANCAM cycles in this explanation are the type described in detail in the LANCAM configuration section on page 9. Lines 16 through 18 perform a LANCAM command read cycle to ensure that any anomalies residing in the LANCAMs after power up are removed before configuration begins. Lines 19 through 26 set the Device Select register to FFFFH to ensure all the LANCAMs respond to subsequent commands. Lines 27 through 34 reset all the LANCAMs by setting the Control registers to 0000H.

Lines 35 through 86 set the Page Address registers of the four LANCAM devices as 00H, 01H, 02H, and 03H. This is done as follows: Lines 35 through 38 targets the Page Address register of the highest-priority (lowest address) device in the chain of four LANCAMs. Lines 39 through 42 set the value of the Page Address register as 00H. Lines 43 through 46 sets the Full flag on this device forcing the next device in the chain to respond to the next set of initialization commands. Lines 47 through 54 targets the highest-priority device again (which is now the second device) and sets the Page Address value as 01H. Lines 55 through 78 continue to set the Full flag of each device and set the page address of the next device until the last device has been set. The last device does not require its Full flag to be set as there are no lower priority devices remaining. Lines 79 through 86 perform a reset forcing the Full flag of all the devices in the chain to their normal function. This reset leaves the recently configured Page Address values unaffected. If only one LANCAM is used, omit lines 43 through 86. If two are used, omit lines 52 through 78 and if three are used, omit lines 67 through 78.

Lines 87 through 134 set the Background registers for use in the purge, set Address register and read entries routines. This is done as follows: Lines 87 through 90 select the Background Register set. Lines 91 through 98 set the Control register to operate with the CAM/RAM partition set for 64 bits of CAM and 0 bits of RAM. It is also set to use Mask Register 1 when doing any comparisons, operate in Enhanced mode, and increment the Address register. Lines 99 through 109 set the persistent destination of subsequent data writes as Mask register 1. Lines 103 through 118 set the Mask register as segment 0 = 7F00H, segment 1 = FFFFH, segment 2 = FFFFH, and segment 3 = FFFFH. This will ensure that only the permanent bit and time stamp bits will be compared during comparisons using the Background Register set.

Lines 119 through 126 set the Segment Control register as follows: When data is written to the LANCAMs, it will be received only in segment 0. When data is read from the LANCAMs, it will be read from segments 0 through 3. Lines 127 through 134 set the persistent source and destination for any future data reads and writes. The Comparand register will receive any data written to the LANCAMs. The memory location specified by the Address register will be the source for any future data that is read from the LANCAMs.

Lines 135 through 182 set the Foreground registers for use in the normal DA and SA filtering routines and for the addition and deletion of permanent entries. This is done as follows: Lines 135 through 138 select the Foreground register set. Lines 139 through 146 set the Control register to operate with the CAM/RAM partition set for 48 bits of CAM and 16 bits of RAM. It also is set not to use any Mask registers when doing comparisons, operate in Enhanced mode, and increment the Address register. Lines 147 through 156 set the Segment Control register as follows: When data is written to the LANCAMs, it will be received in segments 0 through 3. When data is read from the LANCAMs, it will be only read from segment 0. Lines 155 through 158 set the persistent destination of subsequent data writes as Mask register 1. Lines 159 through 174 set the Mask register as segment 0 = 8000H, segment 1 = 0000H, segment 2 = 0000H, and segment 3 = 0000H. This will ensure that the permanent bit is unaltered when the SA filter routine results in MATCH condition. Lines 175 through 182 set the persistent source and destination for any future data reads and writes. The Comparand register will receive any data written to the LANCAMs. The memory location that contains the highest-priority match during the DA filter routine will be the source for any future data read from the LANCAMs.

Lines 183 and 184 set the SLCCS register to 1FH for two cycles. This is to ensure that the LANCAM interface control lines are in a safe state before direct access is turned off. Lines 185 and 186 set the SLCCS register to 0FH for two cycles. This returns control of the LANCAM interface to the MU9C8358L. Line 187 sets the System Target register to increment the STPURG and STCURR registers when the INCR input pin is asserted. It is also set to enable an interrupt on the /INTR output whenever the LANCAMs become full (LANCAM /FF asserted LOW).

Lines 188 through 195 sets the Port Target registers in both devices to allow the MU9C8358L devices to process the SA and DA automatically as they are parsed from incoming packets. The registers also are configured to enable an interrupt when each DA is processed.

Table 6: Initialization and Configuration Routine

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description	Note
1	H	L	01H	0000H	CHIPROL	Configure one device as master	1
2	L	H	01H	0005H	SSCFG	Set static configuration for 70ns CAMs. Also set reject output as active LOW	
3	L	H	0CH	0020H	SMX-SADA CYC	Set the DA/SA cycle time for 70ns CAMs	
4	L	H	02H	0001H	SDCFG	Enable the CAM for normal operation	
5	H	L	40H	0020H	PIDA	Set Port ID for port 0 (in master device)	1
6	H	L	48H	0021H	PIDB	Set Port ID for port 1 (in master device)	1
7	H	L	50H	0022H	PIDC	Set Port ID for port 2 (in master device)	1
8	H	L	58H	0023H	PIDD	Set Port ID for port 3 (in master device)	1
9	H	L	40H	0024H	PIDA	Set Port ID for port 4 (in slave device)	2
10	H	L	48H	0025H	PIDB	Set Port ID for port 5 (in slave device)	2
11	H	L	50H	0026H	PIDC	Set Port ID for port 6 (in slave device)	2
12	H	L	58H	0027H	PIDD	Set Port ID for port 7 (in slave device)	2
13	L	H	12H	000FH	SLCCS	Put CAM output lines into safe mode	
14	L	H	12H	000FH	SLCCS	Wait	
15	L	H	12H	000DH	SLCCS	Preset CAM control lines to initial state	
16	L	H	12H	001DH	SLCCS	Set up command read condition (to clear up any power up anomalies)	
17	L	H	12H	0015H	SLCCS	Take /E bit LOW	
18	L	H	12H	001DH	SLCCS	Take /E bit HIGH	
19	L	H	05H	0228H	SCDW0	Load register with Op-Code: TCO DS	
20	L	H	12H	0019H	SLCCS	Set up command write condition	
21	L	H	12H	0011H	SLCCS	Take /E bit LOW	
22	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
23	L	H	05H	FFFFH	SCDW0	Load register with device: FFFFH = all devices	
24	L	H	12H	0019H	SLCCS	Set up command write condition	
25	L	H	12H	0011H	SLCCS	Take /E bit LOW	
26	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
27	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT	
28	L	H	12H	0019H	SLCCS	Set up command write condition	
29	L	H	12H	0011H	SLCCS	Take /E bit LOW	
30	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
31	L	H	05H	0000H	SCDW0	Load register with code: 0000H=reset all devices	
32	L	H	12H	0019H	SLCCS	Set up command write condition	
33	L	H	12H	0011H	SLCCS	Take /E bit LOW	
34	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
35	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA	
36	L	H	12H	0019H	SLCCS	Set up command write condition	
37	L	H	12H	0011H	SLCCS	Take /E bit LOW	
38	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
39	L	H	05H	0000H	SCDW0	Load register with code: 0000H = set page address of first device	
40	L	H	12H	0019H	SLCCS	Set up command write condition	
41	L	H	12H	0011H	SLCCS	Take /E bit LOW	

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description	Note
42	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
43	L	H	05H	0700H	SCDW0	Load register with Op-Code: SFF	
44	L	H	12H	0019H	SLCCS	Set up command write condition	
45	L	H	12H	0011H	SLCCS	Take /E bit LOW	
46	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
47	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA	
48	L	H	12H	0019H	SLCCS	Set up command write condition	
49	L	H	12H	0011H	SLCCS	Take /E bit LOW	
50	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
51	L	H	05H	0001H	SCDW0	Load register with code: 0001H = set page address of second device	
52	L	H	12H	0019H	SLCCS	Set up command write condition	
53	L	H	12H	0011H	SLCCS	Take /E bit LOW	
54	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
55	L	H	05H	0700H	SCDW0	Load register with Op-Code: SFF	
56	L	H	12H	0019H	SLCCS	Set up command write condition	
57	L	H	12H	0011H	SLCCS	Take /E bit LOW	
58	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
59	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA	
60	L	H	12H	0019H	SLCCS	Set up command write condition	
61	L	H	12H	0011H	SLCCS	Take /E bit LOW	
62	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
63	L	H	05H	0002H	SCDW0	Load register with code: 0002H = set page address of third device	
64	L	H	12H	0019H	SLCCS	Set up command write condition	
65	L	H	12H	0011H	SLCCS	Take /E bit LOW	
66	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
67	L	H	05H	0700H	SCDW0	Load register with Op-Code: SFF	
68	L	H	12H	0019H	SLCCS	Set up command write condition	
69	L	H	12H	0011H	SLCCS	Take /E bit LOW	
70	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
71	L	H	05H	0208H	SCDW0	Load register with Op-Code: TCO PA	
72	L	H	12H	0019H	SLCCS	Set up command write condition	
73	L	H	12H	0011H	SLCCS	Take /E bit LOW	
74	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
75	L	H	05H	0003H	SCDW0	Load register with code: 0003H = set page address of fourth device	
76	L	H	12H	0019H	SLCCS	Set up command write condition	
77	L	H	12H	0011H	SLCCS	Take /E bit LOW	
78	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
79	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT	
80	L	H	12H	0019H	SLCCS	Set up command write condition	
81	L	H	12H	0011H	SLCCS	Take /E bit LOW	
82	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
83	L	H	05H	0000H	SCDW0	Load register with code: 0000H = reset all devices to clear full flags	

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description	Note
84	L	H	12H	0019H	SLCCS	Set up command write condition	
85	L	H	12H	0011H	SLCCS	Take /E bit LOW	
86	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
87	L	H	05H	0619H	SCDW0	Load register with Op-Code: SBR	
88	L	H	12H	0019H	SLCCS	Set up command write condition	
89	L	H	12H	0011H	SLCCS	Take /E bit LOW	
90	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
91	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT	
92	L	H	12H	0019H	SLCCS	Set up command write condition	
93	L	H	12H	0011H	SLCCS	Take /E bit LOW	
94	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
95	L	H	05H	8011H	SCDW0	Load register with code: 8011H = 64 bits CAM, 0 bits RAM, use MR1, Enhanced, increment Address register	
96	L	H	12H	0019H	SLCCS	Set up command write condition	
97	L	H	12H	0011H	SLCCS	Take /E bit LOW	
98	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
99	L	H	05H	0108H	SCDW0	Load register with Op-Code: SPD MR1	
100	L	H	12H	0019H	SLCCS	Set up command write condition	
101	L	H	12H	0011H	SLCCS	Take /E bit LOW	
102	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
103	L	H	05H	7F00H	SCDW0	Load register with code: 7F00H = data write 7F00H to first segment of MR1	
104	L	H	12H	001BH	SLCCS	Set up data write condition	
105	L	H	12H	0013H	SLCCS	Take /E bit LOW	
106	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
107	L	H	05H	FFFFH	SCDW0	Load register with code: FFFFH = data write FFFFH to second segment of MR1	
108	L	H	12H	001BH	SLCCS	Set up data write condition	
109	L	H	12H	0013H	SLCCS	Take /E bit LOW	
110	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
111	L	H	05H	FFFFH	SCDW0	Load register with code: FFFFH = data write FFFFH to third segment of MR1	
112	L	H	12H	001BH	SLCCS	Set up data write condition	
113	L	H	12H	0013H	SLCCS	Take /E bit LOW	
114	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
115	L	H	05H	FFFFH	SCDW0	Load register with code: FFFFH = data write FFFFH to fourth segment of MR1	
116	L	H	12H	001BH	SLCCS	Set up data write condition	
117	L	H	12H	0013H	SLCCS	Take /E bit LOW	
118	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
119	L	H	05H	0210H	SCDW0	Load register with Op-Code: TCO SC	
120	L	H	12H	0019H	SLCCS	Set up command write condition	
121	L	H	12H	0011H	SLCCS	Take /E bit LOW	
122	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
123	L	H	05H	00C0H	SCDW0	Load register with code: 00C0H = write to segment 0, read from segments 0–3	

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description	Note
124	L	H	12H	0019H	SLCCS	Set up command write condition	
125	L	H	12H	0011H	SLCCS	Take /E bit LOW	
126	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
127	L	H	05H	0100H	SCDW0	Load register with Op-Code: SPD CR	
128	L	H	12H	0019H	SLCCS	Set up command write condition	
129	L	H	12H	0011H	SLCCS	Take /E bit LOW	
130	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
131	L	H	05H	0004H	SCDW0	Load register with Op-Code: SPS M@[AR]	
132	L	H	12H	0019H	SLCCS	Set up command write condition	
133	L	H	12H	0011H	SLCCS	Take /E bit LOW	
134	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
135	L	H	05H	0618H	SCDW0	Load register with Op-Code: SFR	
136	L	H	12H	0019H	SLCCS	Set up command write condition	
137	L	H	12H	0011H	SLCCS	Take /E bit LOW	
138	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
139	L	H	05H	0200H	SCDW0	Load register with Op-Code: TCO CT	
140	L	H	12H	0019H	SLCCS	Set up command write condition	
141	L	H	12H	0011H	SLCCS	Take /E bit LOW	
142	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
143	L	H	05H	8041H	SCDW0	Load register with code: 8041H = 48 bits CAM, 16 bits RAM, no mask, Enhanced, increment Address register	
144	L	H	12H	0019H	SLCCS	Set up command write condition	
145	L	H	12H	0011H	SLCCS	Take /E bit LOW	
146	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
147	L	H	05H	0210H	SCDW0	Load register with Op-Code: TCO SC	
148	L	H	12H	0019H	SLCCS	Set up command write condition	
149	L	H	12H	0011H	SLCCS	Take /E bit LOW	
150	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
151	L	H	05H	1800H	SCDW0	Load register with code: 1800H = write to segments 0–3, read from segment 0	
152	L	H	12H	0019H	SLCCS	Set up command write condition	
153	L	H	12H	0011H	SLCCS	Take /E bit LOW	
154	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
155	L	H	05H	0108H	SCDW0	Load register with Op-Code: SPD MR1	
156	L	H	12H	0019H	SLCCS	Set up command write condition	
157	L	H	12H	0011H	SLCCS	Take /E bit LOW	
158	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
159	L	H	05H	8000H	SCDW0	Load register with code: 8000H = data write to 8000H to first segment of MR1	
160	L	H	12H	001BH	SLCCS	Set up data write condition	
161	L	H	12H	0013H	SLCCS	Take /E bit LOW	
162	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
163	L	H	05H	0000H	SCDW0	Load register with code: 0000H = data write 0000H to second segment of MR1	
164	L	H	12H	001BH	SLCCS	Set up data write condition	
165	L	H	12H	0013H	SLCCS	Take /E bit LOW	

Table 6: Initialization and Configuration Routine (continued)

Line	/PCSS	/PCS	A[7:0]	D[15:0]	Register	Description	Note
166	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
167	L	H	05H	0000H	SCDW0	Load register with code: 0000H = data write 0000H to third segment of MR1	
168	L	H	12H	001BH	SLCCS	Set up data write condition	
169	L	H	12H	0013H	SLCCS	Take /E bit LOW	
170	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
171	L	H	05H	0000H	SCDW0	Load register with code: 0000H = data write 0000H to fourth segment of MR1	
172	L	H	12H	001BH	SLCCS	Set up data write condition	
173	L	H	12H	0013H	SLCCS	Take /E bit LOW	
174	L	H	12H	001BH	SLCCS	Take /E bit HIGH	
175	L	H	05H	0100H	SCDW0	Load register with Op-Code: SPD CR	
176	L	H	12H	0019H	SLCCS	Set up command write condition	
177	L	H	12H	0011H	SLCCS	Take /E bit LOW	
178	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
179	L	H	05H	0005H	SCDW0	Load register with Op-Code: SPS HM	
180	L	H	12H	0019H	SLCCS	Set up command write condition	
181	L	H	12H	0011H	SLCCS	Take /E bit LOW	
182	L	H	12H	0019H	SLCCS	Take /E bit HIGH	
183	L	H	12H	001FH	SLCCS	Return LANCAM Interface to inactive	
184	L	H	12H	001FH	SLCCS	Wait	
185	L	H	12H	000FH	SLCCS	Return to Normal	
186	L	H	12H	000FH	SLCCS	Wait	
187	L	H	03H	000EH	STARG	Configure system targets as: INCR input will result in STURR and STPURG increment and a purge. Full Flag will produce an Interrupt on /INTR output	
188	H	L	42H	0060H	PTARGA	Set Port 0 to process DA, SA, and enable interrupts.	1
189	H	L	4AH	0060H	PTARGB	Set Port 1 to process DA, SA, and enable interrupts.	1
190	H	L	52H	0060H	PTARGC	Set Port 2 to process DA, SA, and enable interrupts.	1
191	H	L	5AH	0060H	PTARGD	Set Port 3 to process DA, SA, and enable interrupts.	1
192	H	L	42H	0060H	PTARGA	Set Port 4 to process DA, SA, and enable interrupts.	2
193	H	L	4AH	0060H	PTARGB	Set Port 5 to process DA, SA, and enable interrupts.	2
194	H	L	52H	0060H	PTARGC	Set Port 6 to process DA, SA, and enable interrupts.	2
195	H	L	5AH	0060H	PTARGD	Set Port 7 to process DA, SA, and enable interrupts.	2

Notes:

1. *The MU9C8358L device that is hardware configured as MASTER should be the device that has /PCS asserted LOW during the register write cycle.*
2. *The MU9C8358L device that is hardware configured as SLAVE should be the device that has /PCS asserted LOW during the register write cycle.*

GENERAL LANCAM HOUSEKEEPING

This section shows the steps required when the following operations are performed:

- Add permanent entries to the LANCAMs
- Remove permanent entries from the LANCAMs
- Set the Page Address and actual Address of a LANCAM entry and read it from the LANCAMs
- Maintain the Current Time Stamp and Purge Time Stamp counters
- Initiate the purge routine to delete the oldest entries from the LANCAMs

The MU9C8358L has seven System Command registers (SDO_xxx) that allow a set of built-in LANCAM routines to be invoked. This allows the user to perform LANCAM system management tasks such as adding or removing permanent entries or reading out existing entries. Writing any arbitrary value to the relevant register triggers the routine. Table 7 shows the registers and the built-in routines that they perform. Tables 8 through 14 show how each of the built-in routines are invoked to perform the general management tasks.

48-Bit MAC Address Storage

The two built-in routines that write and delete MAC addresses require the MAC address bits to be arranged in a specific manner. For example, the MAC address 02:60:8C:12:34:56 would be written to the SCDW registers as follows when interpreting Table 8 and Table 9.

SA bits [47:40] = 02

SA bits [39:32] = 60

SA bits [31:24] = 8C

SA bits [23:16] = 12

SA bits [15:8] = 34

SA bits [7:0] = 56

Similarly, when using the appropriate built-in routine to read an entry, Table 9 should be interpreted in the same manner. For example, if the MAC address 02:60:8C:12:34:56 is read from the LANCAM, the 3 16-bit words would be as follows:

CAM seg. 3 = 6002

CAM seg. 2 = 128C

CAM seg. 1 = 5634

Add Permanent Entry

During normal system operation, the MU9C8358Ls will parse incoming packets and automatically add the SAs and their port ID to the LANCAM database. It is also possible to add permanent entries to the LANCAMs manually by invoking a built-in routine as described in Table 8. This is done as follows: Line 1 loads the System CAM Data Word 3 (SCDW3) register with bits 47–32 of the permanent MAC address to be added. Lines 2 and 3 load the remaining MAC address bits into the appropriate SCDW registers. Line 4 loads SCDW0 with the appropriate associated data.

Table 7: System Data Output Registers and Associated Routines

Register	Address	Description of Routine Invoked
SDO_DELETE	20H	Specific MAC addresses may be deleted from the LANCAM database. The user specifies the MAC address by writing it to the SCDW registers, and once triggered, the routine will perform a lookup and delete it.
SDO_ADD	21H	MAC addresses and associated data may be added to the LANCAM database. The user specifies the MAC address by writing it to the SCDW registers, and once triggered, the routine will add it to the next free location in the LANCAM(s).
SDO_READ	24H	Specific MAC addresses may be read from the LANCAM database. The user specifies the LANCAM page address by writing it to SCDW0 and once triggered, the routine will return the 64-bit LANCAM entry and the status information associated with it. The set address (SDO_SETADD) routine must be used prior to this routine being invoked, to specify the LANCAM address.
SDO_INCTS	26H	The Current Time Stamp counter may be incremented using the routine invoked by SDO_INCTS. This will allow the value in the register to be increased to the value that will suit the present network traffic.
SDO_INCPR	27H	The Purge Time Stamp counter may be incremented using the routine invoked by SDO_INCPR. When this routine is invoked, the new value of the Purge Time Stamp counter is compared with the time stamps of the MAC addresses stored in the LANCAM database. All entries that have matching time stamps are deleted. This will allow the value in the register to be increased to the value that will suit the present network traffic.
SDO_INCTSPR	28H	The Current Time Stamp and Purge Time Stamp counters may both be incremented using the routine invoked by SDO_INCTSPR. When this routine is invoked, the new value of the Purge Time Stamp counter is compared with the time stamps of the MAC addresses stored in the LANCAM database. All entries that have matching time stamps are deleted.
SDO_SETADD	29H	The Address register of the LANCAM database may be set to a specific value. This is done prior to the read entry (SDO_READ) routine being invoked.

This will include the Port ID at bits 13–8 and bit 15 set to 1 to indicate a permanent entry. Line 5 triggers the built-in routine by loading the SDO_ADD register with any 16-bit value. When this register is accessed, the MU9C8358L invokes a routine that will take the contents of the SCDW registers and add them to the next free location of the LANCAM database. The entry will not be removed from the database by the periodical purging of older entries and must be removed manually when necessary.

Delete Permanent Entry

Permanent entries will not be removed by the MU9C8358L when the contents of the LANCAM database are periodically purged to remove older entries. Therefore permanent entries must be removed by invoking the delete entries routine as shown in Table 9. Line 1 loads the System CAM Data Word 2 (SCDW2) register with bits 47–32 of the permanent MAC address to be deleted. Lines 2 and 3 load the remaining MAC address bits into the appropriate SCDW registers. Line 4 triggers the built-in routine by loading the SDO_DELETE register with any 16-bit value. When this register is accessed, the MU9C8358L invokes a routine that will take the contents of the SCDW registers and compare the 48-bit MAC address with the contents of the LANCAM database. The matching entry will be deleted.

Read LANCAM Entries

The user may wish to keep track of the active addresses that are stored in the LANCAM database. The system would have to read out entries periodically and store them in a shadow table in the normal system memory. It also may be required to investigate the LANCAM entries to locate information such as a specific Port ID of a known MAC address. To allow the LANCAM entries to be read out, two built-in routines have been provided. When used together in the manner specified, they will set the page address and physical address of the entry and then read the entry and status information. The page address provides the identity of an individual LANCAM if more than one is used in the LANCAM database.

Table 10 shows how the two routines are invoked and is described as follows: Line 1 loads the SCDW0 register with the physical address of the LANCAM entry to be read. Line 2 triggers the built-in routine by loading the SDO_SETADD register with any 16-bit value. When this register is accessed, the MU9C8358L invokes a routine that will take the contents of the SCDW0 register and transfer it to the Address register of the LANCAM Background Register set. When the read entry routine is triggered, the entry that is read is the one specified by the Address register.

Table 8: Adding Permenant Entries Using the Built-In Routine

Line	/PCSS	/WRITE	A[7:0]	D[15:8]	D[7:0]	Register	Description	Note
1	L	L	08H	SA bits [39:32]	SA bits [47:40]	SCDW3	Load register with address bits 47–32	
2	L	L	07H	SA bits [23:16]	SA bits [31:24]	SCDW2	Load register with address bits 31–16	
3	L	L	06H	SA bits [7:0]	SA bits [15:8]	SCDW1	Load register with address bits 15–0	
4	L	L	05H	aaH	aaH	SCDW0	Load register with associated data	1
5	L	L	21H	xxH	xxH	SDO_ADD	Trigger the add entry routine	2

Notes:

1. *aa = The associated data of the MAC address. This has bit 15 set to 1 to indicate a permanent entry and bits 13–8 set to indicate the Port ID.*
2. *xx = "Don't care"*

Table 9: Deleting Permenant Entries Using the Built-In Routine

Line	/PCSS	/WRITE	A[7:0]	D[15:8]	D[7:0]	Register	Description	Note
1	L	L	07H	SA bits [39:32]	SA bits [47:40]	SCDW2	Load register with address bits 47–32	
2	L	L	06H	SA bits [23:16]	SA bits [31:24]	SCDW1	Load register with address bits 31–16	
3	L	L	05H	SA bits [7:0]	SA bits [15:8]	SCDW0	Load register with address bits 15–0	
4	L	L	20H	xxH	xxH	SDO_DELETE	Trigger the delete entry routine	1

Notes:

1. *xx = "Don't care"*

Line 3 loads the SCDW0 register with the page address of the LANCAM to be read. This specifies the actual LANCAM device, which is to be selected when a chain of multiple devices is used. The value loaded into the SCDW0 register would be one of the values configured during the Configuration routine. If only one LANCAM is used, the page address should be 00H. Line 4 triggers the built-in routine by loading the SDO_READ register with any 16-bit value. When this register is accessed, the MU9C8358L invokes a routine that will take the contents of the SCDW0 register and transfer it to the LANCAM Page Address register. The 64-bit entry specified by the LANCAM Address and Page Address registers is transferred to the SCDW registers of the MU9C8358L. The 32-bit LANCAM Status register is transferred to the SCSWA and SCSWB registers of the MU9C8358L.

Lines 5 through 8 read the specified LANCAM entry from the SCDW registers. Lines 9 through 10 read the LANCAM status bits from the SCSWA and SCSWB registers. The 32-bit Status Register value indicates the validity of the entry in bits 29–28. Therefore, if this information is the only status detail that is required, line 10 may be omitted. Please refer to the appropriate LANCAM Family data sheet for a full description of the status bits. If a block of entries and their status is to be read sequentially, lines 3 through 10 may be repeated until all the entries have been read. Lines 1 and 2 do not have to be repeated for each entry as the LANCAM Address register automatically increments.

Purge Older Entries

The MU9C8358L has two counters that are used when adding time stamps and removing older entries. The first of these counters is the Current Time Stamp counter (STCURR). This 8-bit counter provides 256 possible time stamp values that are added to the associated data field during the SA lookup operation. When the SA lookup routine is performed by the MU9C8358L, the 8-bit value of STCURR is automatically added to bits 7–0 of the LANCAM associated data field (bits[15:0]). The second of these counters is the Purge Time Stamp counter (STPURG). This 8-bit counter stores the present purge value. When a purge routine is initiated, this counter is incremented. The value in it is then compared with the 8-bit time stamp value stored with every nonpermanent entry in the LANCAM database. Matching entries are subsequently deleted and are therefore purged or aged out.

Table 10: Reading Entries Using the Built-In Routine

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	05H	CAM address	SCDW0	Load register with address of entry	
2	L	L	29H	xxxxH	SDO_SET ADD	Trigger the set address routine	1
3	L	L	05H	Page address	SCDW0	Load register with page address of entry	
4	L	L	24H	xxxxH	SDO_ READ	Trigger the read entry routine	1
5	L	H	08H	CAM seg. 3	SCDW3	Read the specified LANCAM entry (bits 63–48) from SCDW3	
6	L	H	07H	CAM seg. 2	SCDW2	Read the specified LANCAM entry (bits 47–32) from SCDW2	
7	L	H	06H	CAM seg. 1	SCDW1	Read the specified LANCAM entry (bits 31–16) from SCDW1	
8	L	H	05H	CAM seg. 0	SCDW0	Read the specified LANCAM entry (bits 15–0) from SCDW0	
9	L	H	0DH	Status bits [31:16]	SCSWB	Read the LANCAM status bits 31–16 from SCSWB	
10	L	H	0EH	Status bits [15:0]	SCSWA	Read the LANCAM status bits 15–0 from SCSWA	

Notes:

1. xxxx = "Don't care"

For example, Figure 6 shows some of the possible settings of both STCURR and STPURG. Item 1 shows both counters set for a very small data-age gap. An entry would exist in the database for 30 purge intervals only, if it were not updated before its time stamp equals STCURR. Item 2 shows a medium data-age gap of 120 and item 3 shows the maximum gap, which is 255. Using item 2 as an example, the purge sequence operates as follows:

1. After a purge of older entries is triggered, both counters are incremented, which will make STPURG = 2FH and STCURR = A7H. During the time interval between now and when the next purge is triggered, all the time stamps that are added or updated will equal A7H.
2. The new value of STPURG (2FH) is compared with all the entries in the LANCAM database. All the entries with the same value as STPURG and not marked as permanent are deleted. Therefore, if the data-age gap remains constant, any entries added to the database will remain undeleted for at least 120 purges.

Three built-routines (as shown in Tables 11 through 14 on page 23) are provided to adjust the counter values and to initiate the purge sequence. The first of these routines is the increment time stamp routine and is triggered by writing to the SDO_INCTS register. This adjusts STCURR by adding one to the present value and is used to increase the time entries exist in the LANCAM database. Because STCURR and the STPURG are both 8 bits wide, 256 possible time stamps are possible. By incrementing STCURR, the difference between it and STPURG can be increased and therefore increase data-age gap from anything between 1 and 255 purge intervals. A purge interval would be the time interval between the CPU initiating its regular purge of older entries (described later).

The second routine is the increment purge time stamp routine and is triggered by writing to the SDO_INCPR register. This adjusts STPURG by adding one to the present value and then comparing the new value with bits 7–0 of each nonpermanent entry in the LANCAM database. Matching entries are deleted and removed from the database. By incrementing STPURG, the difference between it and STCURR can be decreased and therefore decrease the time that entries in the LANCAM database will exist.

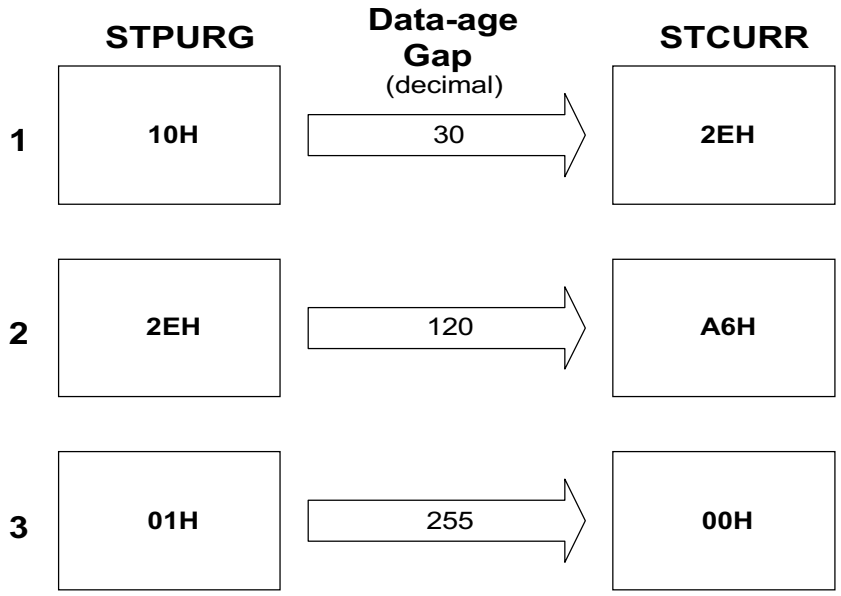

Figure 6: Examples of STCURR and STPURG Settings

The SDO_INCTS and SDO_INCPR routines should be used to adjust STCURR and STPURG and therefore adjust the data-aging rate. By monitoring network traffic density, the difference between the two counters can be increased or decreased to suit. As traffic flow decreases, increasing STCURR (as shown in Table 11) can increase the difference between the counters. This will ensure entries are aged out less frequently. Conversely as traffic flow increases, increasing STPURG (as shown in Table 12) can reduce the difference between the counters. This will ensure that entries are aged out more frequently. It is important to note that the value of STCURR should never be left with the same value as STPURG.

Using the SDO_INCPR routine can be used for more than altering the data-aging rate. It can be used in severe conditions when the LANCAM database becomes full to remove older entries and increase the data-aging gap. When this condition exists, the /INTR output is asserted by the MU9C8358L (if configured in STARG) to indicate an interrupt. The CPU must then read the System Status (SSTAT) register to confirm the cause of the interrupt. The SDO_INCPR can be invoked to remove some of the entries from the database. It cannot be assured that initiating a single purge of older entries will actually delete anything, because there may be no entries in the database that have the same time stamp value as the one to be purged. Therefore, it is recommended that the purge routine is invoked repeatedly until an entry or entries have been deleted. The SSTAT register must be monitored after invoking the SDO_INCPR routine to check if the LANCAM /FF has returned to its normal status. Table 13 shows how the SDO_INCPR can be used to remove entries in this way. Lines 1 and 2 can be repeated until sufficient entries have been deleted from the database.

The third routine is the increment time stamp and purge time stamp counters routine and is triggered in two ways. It can be triggered by writing to the SDO_INCTSPR register or by asserting the INCR hardware input (if it is configured in the STARG register). This built-in routine is used for the normal purging or aging out of older entries. The routine will increment both the STCURR and STPURG counters (and therefore keep the data-aging gap constant) and also delete any matching LANCAM entries as described earlier. The CPU should perform this task at regular intervals to remove older entries from the database.

Table 11: Increasing the Value of STCURR to Decrease the Data-aging Gap

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	26H	xxxxH	SDO_INCTS	Trigger the increment STCURR sequence	1

Table 12: Increasing the Value of STPURG to Increase the Data-aging Gap

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	27H	xxxxH	SDO_INCPR	Trigger the increment STPURG sequence	1

Table 13: Invoke the Increment STPURG Sequence to Purge Older Entries

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	27H	xxxxH	SDO_INCPR	Trigger the increment STPURG sequence	1
2	L	H	00H	Status bits Bit 0 = /FF	SSTAT	Read the SSTAT register to identify condition of LANCAM Full flag	2

Table 14: Invoke the Increment STPURG and STCURR Sequence to Purge Older Entries

Line	/PCSS	/WRITE	A[7:0]	D[15:0]	Register	Description	Note
1	L	L	28H	xxxxH	SDO_INCTSPR	Trigger the increment time stamp and purge sequence	1

Notes:

1. *xxxx = "Don't care"*
2. *The SSTAT register has the status of the LANCAM Full flag in bit 0. If bit 0 = 0, the LANCAM is full and if bit 1 = 1, the LANCAM has at least one empty location. Bits 15– 1 can be ignored during the register read.*

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