Implementing An ARP Cache Using The MUAA™ CAM Family

INTRODUCTION

Content-addressable memory (CAM) has many advantages that make it superior to software solutions in today's high speed networking applications. The MUSIC MUAA CAM Series uses well established CAM technology combined with time saving enhancements to make it the ideal choice for implementing an ARP cache. The advantages are:

- Fast deterministic address translation
- A comprehensive instruction set that includes search, learn and delete operations for ease of use
- Automatic aging functions remove the need for external management software
- Reduced ARP traffic: a fast CAM can build an ARP table by snooping on data packet headers

The Internet Protocol (IP) address of a node is a software-assigned set of numbers used in layer 3 packet transportation. The "actual" or physical address that the data link layer (layer 2) knows for a node is the hardware, or MAC address. This address is unique to each node and is usually set in hardware on the interface card by the manufacturer or configured from a list by a system administrator.

Before any data transfer can occur, an address translation must be performed to convert an IP address to its corresponding MAC address. The Address Resolution Protocol (ARP) handles this translation of IP addresses to their physical addresses. ARP uses a translation table which is referred to as ARP cache. The table contains mappings of specific layer 3 addresses to their corresponding layer 2 hardware addresses.

The majority of ARP translations performed are from IP addresses to Ethernet addresses. Therefore the MUSIC MUAA CAM provides an ideal solution for the implementation of an ARP cache. It can store 80-bit entries, which will accommodate both the 32-bit IP address and its corresponding 48-bit Ethernet MAC address. The MUAA CAM performs all of the operations required by ARP such as search, insert, and delete.

Software techniques, such as sorted trees or hashing, even when implemented as hardware Finite State Machines, do not have deterministic search times. Such techniques require complex time-consuming maintenance and management, particularly when adding or deleting entries. Alternatively, the MUAA CAM always gives the desired translation in a fast, deterministic way and requires no special sorting when adding or deleting entries. Using a 50MHz clock input, ARP translation requires only 80ns.

An important advantage is gained by implementing an ARP cache using the MUAA CAM Family. Because searches and insertions can be performed more quickly and efficiently with a CAM than with software, ARP traffic can be greatly reduced. If new entries are added to the cache at each arriving packet, nodes will therefore need to send less ARP traffic in order to make updates.

The MUAA CAM memory array can be partitioned into separate CAM and RAM memory blocks. This feature allows the IP addresses to be stored in the 32-bit CAM partition and the corresponding 48-bit Ethernet address stored in the RAM partition. When searching for appropriate translation data, the IP address is written to the CAM and if a match is found, the required Ethernet address is given.

If the hardware performing the address resolution requires a translation from a 32-bit address to more than 48 bits, this also is possible with the MUAA CAM. An example of this would be to append an Ethernet Destination Address, Source Address, and Frame Type directly to the outgoing frame. After the IP address search produced a match, the MUAA CAM can output an index that will directly address external memory. This external memory would store the frame headers, which would be appended before transmission.

ARP caches are usually refreshed at regular intervals to deal with changes in network topology. By removing entries from the cache that have not been selected recently, the transmitting node can be sure that the translated hardware address is up to date. Therefore the ARP cache should

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always only contain correct, up to date translations. An external software process would normally be required to refresh the translation table. The MUAA CAM has the facility to perform all the time stamping and aging functions, required for refreshing the cache, automatically. This will take the load off external software and increase the ease of design.

THE ADDRESS RESOLUTION PROTOCOL

The Address Resolution Protocol (ARP) defines a broadcast-based method for dynamically translating between higher level addresses and physical addresses. Although many different network layer protocols and hardware methods are defined, the most common case is translating between IP and Ethernet. Before a network node can transmit data to another node, a translation must take place. The higher level software of the transmitting node will only know the destination by its layer 3 address. Therefore the Network Interface Card (NIC) must prefix the physical MAC address (layer 2) to the packet before transmission. To do this, the NIC uses the ARP to translate the software address to its hardware address.

An ARP cache or translation table is used to store known layer 3 addresses and their associated layer 2 addresses. This would normally be located on the NIC or managed by the NIC software driver and is continually updated when new translations are learned. When a node wants to transmit data it will first check the ARP cache to find the physical address of the destination node. If the cache contains the address, it can be appended to the packet and transmitted. If the translation is not held in the cache, an ARP request is issued and the reply is used to update the translation table.

To explain how this mechanism works, a small network with three nodes will be used as an example. Figure 1 shows a very simple Ethernet LAN with three computers sharing the transmission medium and using IPV4 as the layer 3 protocol. If node A wants to send information to node C it will search the cache for the physical address of node C. Assuming that the translation data is not found, it will issue an ARP request. An ARP request is a special broadcast packet that is sent to all the nodes on the network. This will inform all the nodes that node A is wishing to send data to the node with the IP address of node C.

Both nodes B and C would receive the broadcast ARP request packet sent by node A. Node B would examine the packet but would not respond to it after it found the Destination IP Address differed from its own. At this point, node B would be able to use the data contained in the ARP request if it wanted to update its own translation table. The intended recipient, node C, would respond to the request by sending an ARP reply back to node A. This would contain the address translation information for nodes A and C.

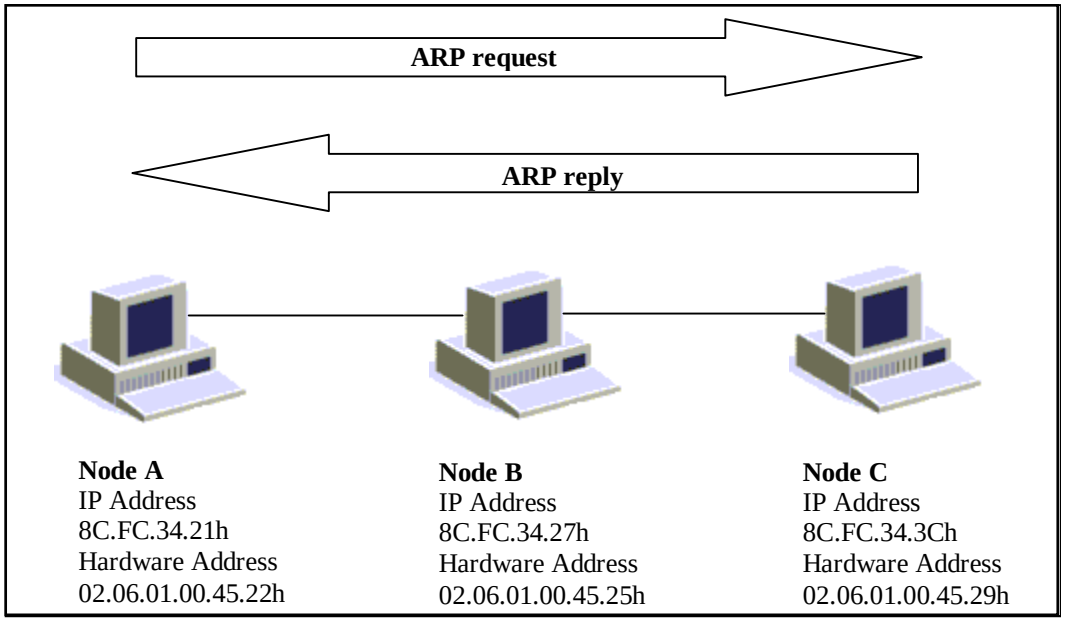

Figure 1: A Simple Three Node Ethernet LAN

Hardware Type (16 bits)	
Protocol Type (16 bits)	
Hardware Address Length (8 bits)	Protocol Address Length (8 bits)
Operation Code (16 bits)	
Source Hardware Address	
Source Higher Layer Address	
Destination Hardware Address	
Destination Higher Layer Address	

Table 1: ARP Request and Reply Layout

This mechanism allows not only the transmitting node to update its cache, but also the receiving node. Node C can now update its ARP cache with the newly learned IP and hardware address of node A. When the ARP reply is received by node A, it will use the translation data to allow it to transmit the data destined for node C. It can also update its ARP cache with the new address information. This will remove the need for further unnecessary ARP request traffic caused by subsequent data transfer between nodes A and C. The layout of an ARP request and reply is shown in Table 1. The size of the last four fields varies depending upon which translation is required. For translation between an IP Address and an Ethernet Hardware address, the higher layer and hardware field sizes would be 32 bits and 48 bits respectively.

The ARP fields are described in Table 2. These fields are encapsulated within the data portion of the transmitted request or reply packet. The request is issued as a broadcast packet from node A and will be received by all of the nodes on the network. The format of the ARP request packet can be seen in Figure 2. The reply is sent from the responding node (which was C) to the node that issued the request (which was A). The format of this packet can be seen in Figure 3.

USING THE MUAA CAM AS AN ARP CACHE

CAM provides a system designer with a fast and efficient alternative way to implement an ARP cache. In today's high-speed routers and servers address resolution must be performed with as little time overhead as possible. Normally software techniques such as binary trees and hashing would be used to store and search the translation data that would constitute the cache. Adding entries to the table would involve complex, time consuming management routines, as a degree of sorting would be required. Likewise, the time taken to locate the associated match data would also be time consuming and vary from search to search.

By using a CAM to store the address resolution entries, a system designer can produce a fast, efficient, deterministic ARP cache. The entries can be stored anywhere in the memory array and hence remove the need for complex management routines. Due to the fact that all the entries are compared simultaneously, the result is always available after one fast operation. Because of the small time overhead required to add entries, the ARP cache can be updated when packets are received, thus reducing unwanted ARP traffic.

	Description
Protocol Type	This specifies the higher level protocol being used. For example IP, X.25 Level 3 and DEC DECNET, etc.
Hardware Type	This specifies the type of hardware being used. Examples of hardware used are Ethernet, Token Ring, Local Talk, and Frame Relay.
Hardware Address Length	This specifies the hardware address length (in bytes). For Ethernet this would be set to 6.
Protocol Address Length	This specifies the higher level protocol address length (in bytes). For IP this would be set to 4.
Operation Code	This is set to 0001h for an ARP request and 0002h for an ARP reply.
Source Hardware Address	This is the physical address of the node sending the request or reply. For example, this would contain the Ethernet MAC Address of the transmitting node.
Source Higher Layer Address	This is the higher layer address of the node sending the request or reply. For example this would contain the IP Address of the transmitting node.
Destination Hardware Address	This is the physical address that an ARP request is trying to locate and would be left as 0. In a reply this would contain the physical address of the node that the reply is being sent to. In our example this would be an Ethernet MAC Address.
Destination Higher Layer Address	In a request, this is the higher layer address that needs to be translated. In a reply, this is the higher layer address of the node that sent the initial request. For example this would contain an IP Address.

Table 2: Description of the Fields Used in an ARP Request and Reply

Preamble	Destination Address	Source Address	Type	ARP Request Data	FCS
	FF.FF.FF.FF.FF.FFh	02.06.01.00.45.22h	0806h		

Hard Type	Prot Type	Hard Size	Prot Size	Op code	Ethernet SA	Source IP Address	Ethernet DA	Destination IP Address
0001h	0800h	06h	04h	0001h	02.06.01.00.45.22h	8C.FC.34.21h	0h	8C.FC.34.3Ch

Figure 2: Format of the ARP Request Broadcast Packet from Node A

Preamble	Destination Address	Source Address	Type	ARP Request Data	FCS
	02.06.01.00.45.22h	02.06.01.00.45.29h	0806h		

Hard Type	Prot Type	Hard Size	Prot Size	Op code	Ethernet SA	Source IP Address	Ethernet DA	Destination IP Address
0001h	0800h	06h	04h	0002h	02.06.01.00.45.29h	8C.FC.34.3Ch	02.06.01.00 .45.22h	8C.FC.34.21h

Figure 3: Format of the ARP Reply Sent from Node C to Node A

The MUSIC MUAA CAM Family has many features that will allow it to be used easily as an ARP cache. One of these features is the ability to partition the memory array into separate CAM and RAM areas. The CAM partition is the part of the field that the IP addresses will be stored. The RAM partition is the part of the field that contains associated Ethernet address. MUAA CAMs have an 80-bit wide memory array, which can be programmable from 32 bits of CAM and 48 bits of associated data, to 80 bits of CAM and 0 bits of RAM. In a typical IP to Ethernet ARP cache application, it is partitioned as 32 bits of CAM and 48 bits of RAM. This sets the CAM partition wide enough to accommodate the 32-bit IP addresses. The remaining 48 bits of the word will be used for the associated 48-bit Ethernet MAC addresses.

When a search is undertaken in order to perform the ARP translation required by the transmitting node, the 32-bit IP address is compared simultaneously with all the valid entries in the partitioned 32-bit CAM area. If the IP address is already stored in the ARP cache, the associated Ethernet address will be accessible from the device in a fast deterministic manner. The comparison will always take 80ns when using a 50MHz-clock input, regardless of how many entries are stored in the cache. If the associated Ethernet address is all that is required it could be read from the RAM partition of the device in two cycles. Figure 4 shows how the MUAA CAM is partitioned to hold IP to Ethernet translation information.

The MUAA has the ability to allow an address index to be given when there has been a successful comparison. This is the match-address where the IP address was located and can be used to index an additional area of RAM. This external RAM area can then be used to store further associated data other than the corresponding 48-bit Ethernet address. An example of this would be to store complete frame headers in an external RAM. The frame headers would consist of the Ethernet destination address, source address and frame type, which can be directly appended to an outgoing frame. The address index can be configured to be available before or after the associated RAM partition to allow complete flexibility when allocating associated data width.

Time stamping and aging is used to refresh the ARP cache on a regular basis. This is to ensure that nodes that no longer exist or have been reconfigured are removed or updated. When a conventional CAM is used, extra bits of associated data would be required to implement the aging scheme. It would also increase the time required to add or update entries. This complication is removed when using the MUAA CAM as all the entries are automatically aged. This is explained later in the section on time stamping and aging on page 8.

The MUAA CAM has two ports for data transfers to and from the device. This will give the system designer access to the table entries directly in hardware or by using higher level software through the system microprocessor bus architecture. The two ports are the synchronous port and the processor port. Operations may occur on both ports at the same time; the port with the highest-priority will gain CAM access first if both ports require a read or write into the CAM array simultaneously. The port priority would be set during the configuration routine. Figure 5 shows the typical block diagram of how the MUAA CAM I/O ports would be interfaced.

Synchronous Port

The synchronous port consists of DIN(31:0), DOUT(31:0), and the associated inputs and outputs required for successful data transfer. Setting or clearing bit 1 and bit 2 in the Configuration register can configure it for either 16-bit or 32-bit use. The control hardware will transfer data to the CAM by loading it onto the DIN(31:0) pins of the CAM (and take /DINE LOW). At the same time, the correct instruction is given by loading the OP(3:0) pins with the appropriate data. There is a range of instructions possible such as learn, search, delete, load, and age. For example, loading DIN with the 32-bit IP address carries out a translation search when the search or searcha instruction is given. The full list of all the possible instructions with an explanation of their use can be found in the MUAA CAM data sheet. A full description of all the operations that are required is given later in the CAM Code section on page 10.

Data is transferred from the CAM to the control hardware using the DOUT(31:0) output of the synchronous port. The CAM will load the DOUT(31:0) pins with the relevant data and take /DOUTVALID LOW. Please note that the timing of /DOUTVALID with respect to DOUT(31:0) can be configured to be active on the same CLK or one CLK period earlier. This will allow the MUAA CAM to be interfaced with devices that have registered I/O.

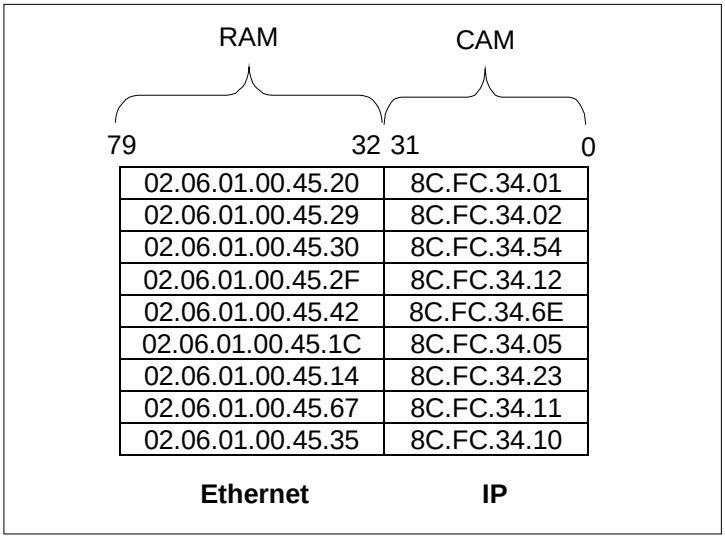

Figure 4: MUAA CAM Partioned for IP to Ethernet Translation

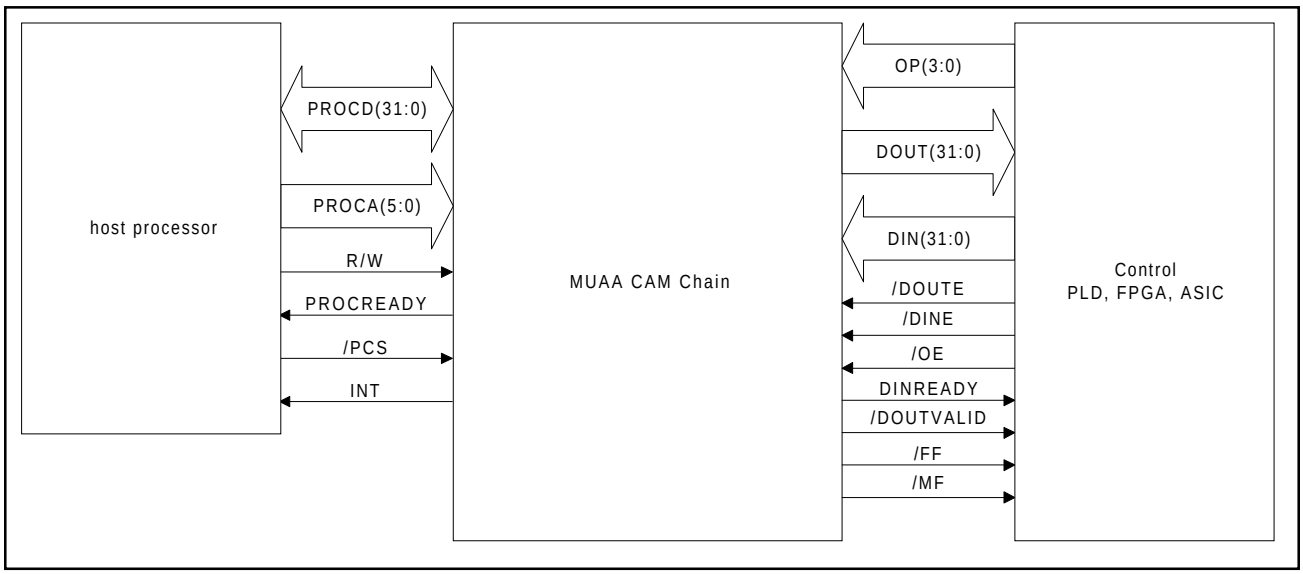

Figure 5: C Block Diagram Showing MUAA CAM I/O Ports

The output port is used to transfer the associated data (corresponding Ethernet address) and address index. The address index will allow the user to implement further associated data in software or hardware if so required. This can be configured to be available before or after the associated data, when a IP search results in a MATCH condition. At this point both the associated data and the address index will become available. If the address index is not required, the associated data should be configured to become available first, which will output the corresponding Ethernet address.

The user has high impedance control of the output data from the synchronous port by asserting /OE when necessary. The /DOUTE input is the DOUT(31:0) enable control. When the data word is configured to be wider than the output port, this strobe enables the next word(s) of the DOUT data onto the DOUT(31:0) pins. This will be required when reading the 48-bit Ethernet addresses after a successful search as two cycles are required. The input and output ports could share the same 32 bit or 16 bit bus, allowing the pin count of surrending hardware to be reduced if required. Refer to the MUAA CAM data sheet for a comprehensive description of all the pins found in the MUAA CAM Family.

Processor Port

The processor can transfer data to the CAM by loading the PROCD(31:0) pins with the necessary data. These pins are bi-directional and are used for both reading and writing to the CAM. The internal registers are accessed by the use of the PROCA (5:0) inputs. The relevant address is loaded on Bits 5–1 with Bit 0 being used only in 16-bit mode. When 16-bit mode is selected, a logic 0 indicates the lower 16 bits of the register and a logic 1 indicates the upper 16 bits. But if a 32-bit mode is selected, Bit 0 must be connected to a valid logic level. The processor has other pins that are required to ensure successful data transfer. These are R/W, /PCS, and PROCREADY.

R/W is a read or write input that controls the direction of data to and from the CAM. R/W is held LOW to write data to the CAM and it is held HIGH to read data from the CAM. /PCS is the processor port chip select input and is asserted LOW to indicate that the cycle is to the processor port. The relevant timing information for read and write cycles with respect to /PCS are given in the MUAA CAM data sheet. PROCREADY is an output from the CAM and indicates that the processor may read data or data was successfully read by the device.

Interface Pins

The MUAA CAM Family has other pins that allows it to be interfaced simply with surrounding hardware. /MF is the Match Flag output and is asserted LOW by the device to indicate that there was a match after the previous search or learn operation. /FF is the Full Flag output and is asserted LOW by the device to indicate that the device is full and is unable to learn new addresses. CHAINUP, CHAINDN, CHAINCS, and CHAIN(3:0) allow up to four CAMs to be transparently chained together. See the section on device chaining on page 10 for more information.

The CAM has an INT output pin which is asserted HIGH or LOW (this is configured to suit the users application). This allows hardware to be notified of any internal interrupts. The four interrupts that are possible are the aged or learn queue has at least one entry, or a processor or synchronous write exception has occurred. The individual interrupts can be enabled or disabled at system configuration. When enabled, the interrupt facility allows the system to keep track of aged and learned entries, and to deal with exceptions.

The CLK input is the main system clock and registers all data read and writes to the device. /RESET is the system reset input. This must be asserted LOW for at least 3 CLK periods to reset the MUAA CAM. Please note that the DINREADY output may stay LOW for up to 800 CLK periods after /RESET has been taken HIGH. /TRST, /TCLK, TMS, TDI, and TDO are the JTAG IEEE Standard test pins.

AQUEUE and LQUEUE

The MUAA CAM Family provides “virtual queues” to enable the system to keep track of entries that are aged or learned. The AQUEUE contains all entries that have been aged from the CAM memory array. The LQUEUE contains all the entries that have been learned or added to the CAM memory array. Both “virtual queues” work in the same way with only minor differences. The LQUEUE is always enabled whereas the AQUEUE must be enabled, if it is required, by setting bit 14 of the Configuration register to 1. Both share the same hardware interrupt output (INT) to inform the processor that a new entry has been written into the relevant queue.

These interrupts are enabled or disabled in the Configuration register. When an interrupt occurs, the MUAA CAM asserts the INT pin. The system can find the cause by reading the Address Index register and acknowledge it by reading the appropriate Flag register. The interrupt will not be re-asserted until the relevant queue has been emptied and then receives another entry. The Flag registers can also be used in a software implementation when the INT pin is not enabled.

The entries in the queues can be read out from the processor port using the read LQUEUE and read AQUEUE instructions. This would allow the upper level software access to the information regarding the age of entries when using the auto-age facilities. Although the MUAA CAM will automatically age the entries in the cache to refresh the table and reduce transmission errors, higher level software may need to be informed of the aging status. When attempting to read queue entries from the processor port, there may be a delay if the synchronous port has higher priority and is also accessing the CAM memory array. For example, if the processor port tries to gain access to read a queue entry, the PROCREADY output would be held LOW by the MUAA CAM until the synchronous port was finished. The PROCREADY would then be taken HIGH to indicate that the data read operation could be completed. Both queues can also be completely emptied by using the appropriate clear instruction.

SWEX and PWEX

The MUAA CAM series contains two interrupts that signal write exceptions. The exceptions indicate that a lower priority port attempted to write a new entry into the CAM at the same time as the higher priority port, when the higher priority port already has a write operation in the pipeline and the CAM has 2 entries left. The SWEX exception indicates that the synchronous port was the offending lower priority port and PWEX indicates the processor port.

Both interrupts will cause the INT pin to be asserted if they are enabled in the Configuration register. The interrupt service routine should read the Address Index register to identify the cause of the interrupt. The appropriate Flag register should then be read to acknowledge the interrupt and return the INT pin to its normal state. Appropriate action can then be taken to rectify the subsequent problems caused by the exception.

For instance, assuming that the synchronous port has been configured to be the highest-priority, the INT pin is asserted if the processor port causes an exception. Once the PWEX Flag register has been read to acknowledge the interrupt and reset the INT output, the following action can be taken. The learn or insert instruction initiated by the processor prior to the exception must be attempted once the MUAA CAM is no longer full. The /FF output can be monitored to notify the processor when the MUAA CAM is no longer full and hence allow it to re-attempt the failed instruction. Issuing a manual age instruction may require a deletion of some older entries and therefore producing some free memory space.

TIME STAMPING AND AGING

Normally software techniques are used to mark the entries in the translation table with a time stamp in order to keep track of the age of an entry. As new entries are added, the associated data field would be used to store the time stamp as well as other necessary information. Entries could also be marked as static or permanent. The software routines would normally use simple “old” and “new” time stamps or a more sophisticated approach with multiple time-stamps. The more sophisticated approach would give the entries a range of time stamps and age out the oldest when necessary.

When a search (in order to find an associated Ethernet address) produces a MATCH condition, the associated data field would be updated to contain the most recent time-stamp. If the search produced a NO-MATCH condition the ARP request and reply operation would be performed in order to update the cache. The newly learned IP address and its Ethernet address would then be added to the memory array with its time stamp. After a predefined aging interval, the processor would then invoke a purge routine to remove all the entries that contain the oldest time stamp (permanent entries would not be removed). This would help network management as nodes, that no longer exist or have been reconfigured, would be automatically removed from the table. This would help reduce transmission errors caused by packets being sent to the wrong address.

Automatic Aging with the MUAA CAM

The MUAA CAM Family has an IEEE compliant automatic time stamp and aging facility that greatly increases the usability of the device. The time stamps are stored internally when entries are learned and are invisible to the user. The auto-aging function is selected by setting bit 13 of the Configuration register to 1. This will cause the CAM to automatically purge or delete all entries in the CAM that have the oldest time stamp (and are not marked permanent). The oldest entries can also be aged out manually (whether or not auto-aging is enabled) by using the age instruction. The auto-age interval is the time that will elapse between purges and is configured by the user by setting the Auto-age Interval register. The register is 32 bits wide and the value contained in it is divided by the CLK input to produce

AUTO-AGING

REGISTER	BIT	VALUE	DESCRIPTION	NOTES
Configuration register	13	1	Turns the auto-aging function on.	
Configuration register	18	1 or 0	Sets the priority of auto-age over I/O ports.	1
Auto-age Interval register	all	32-bit value	This sets the time between the automatic aging.	2
Learned Entry Life register	all	9-bit value	This sets the length of the entry life.	3

MANUAL AGING

REGISTER	BIT	VALUE	DESCRIPTION	NOTES
Configuration register	13	0	Turns the auto-aging function off.	
Configuration register	18	Don't care	This bit sets the priority of auto-aging. Because auto-aging is off, this can be either 1 or 0.	
Auto-age Interval register	all	Don't care	This sets the time between purges. Because auto-aging is off, this can be left with its initial value.	
Learned Entry Life register	all	9-bit value	This sets the length of the entry life.	3

NOTES:

1. When the auto-aging function is chosen, the priority must be set. At some point the auto-age logic may want to operate at the same time as the synchronous or processor ports. Setting bit 18 of the Configuration register to 1 gives the auto-age function higher priority. In a typical bridge or switch application this bit would be set to 0 to give the function the lowest priority.
2. The Auto-age Interval register requires a 32-bit value to set the interval between purges or aging. This value is divided by the system input CLK signal to produce the time interval. The MUAA CAM Series resets with the value 02FAF080h in this register. If a 50MHz CLK signal is used, the aging interval will be one second.
3. The Learned Entry Life register requires a 9-bit value to set the length of time each entry will exist in the CAM if it is not updated. This is effectively the number of aging intervals that will occur before the entry will expire. The life of each entry will restart very time it is 'touched' or the time-stamp is updated. The system resets with the value 012Ch, giving each entry a life of 300 seconds with a 1-second aging interval.

Table 3: Register Settings for Automatic and Manual Aging

the time interval. The register resets to 02FAF080h, which will give an interval of 1 second with a 50MHz CLK.

The priority of this auto-aging function is selected at configuration. The value of bit 18 in the Configuration register is changed to make automatic aging higher or lower-priority than synchronous or processor port operations. In a typical ARP cache, any auto-aging facility would normally be given the lowest-priority. The time stamps are automatically added or updated when an IP/Ethernet search or addition is carried out. The **searcha<DIN>** instruction is used to search the CAM array for the corresponding Ethernet address. The **learn<DIN>** instruction is used to add new translation data to the cache. Both instructions will automatically add or update the time-stamp associated with the entry.

Table 3 shows the different settings required for automatic and manual aging. If the user does not want to use the time stamp and aging facility, the CAM would be configured as for no automatic aging and the manual age instruction would never be given.

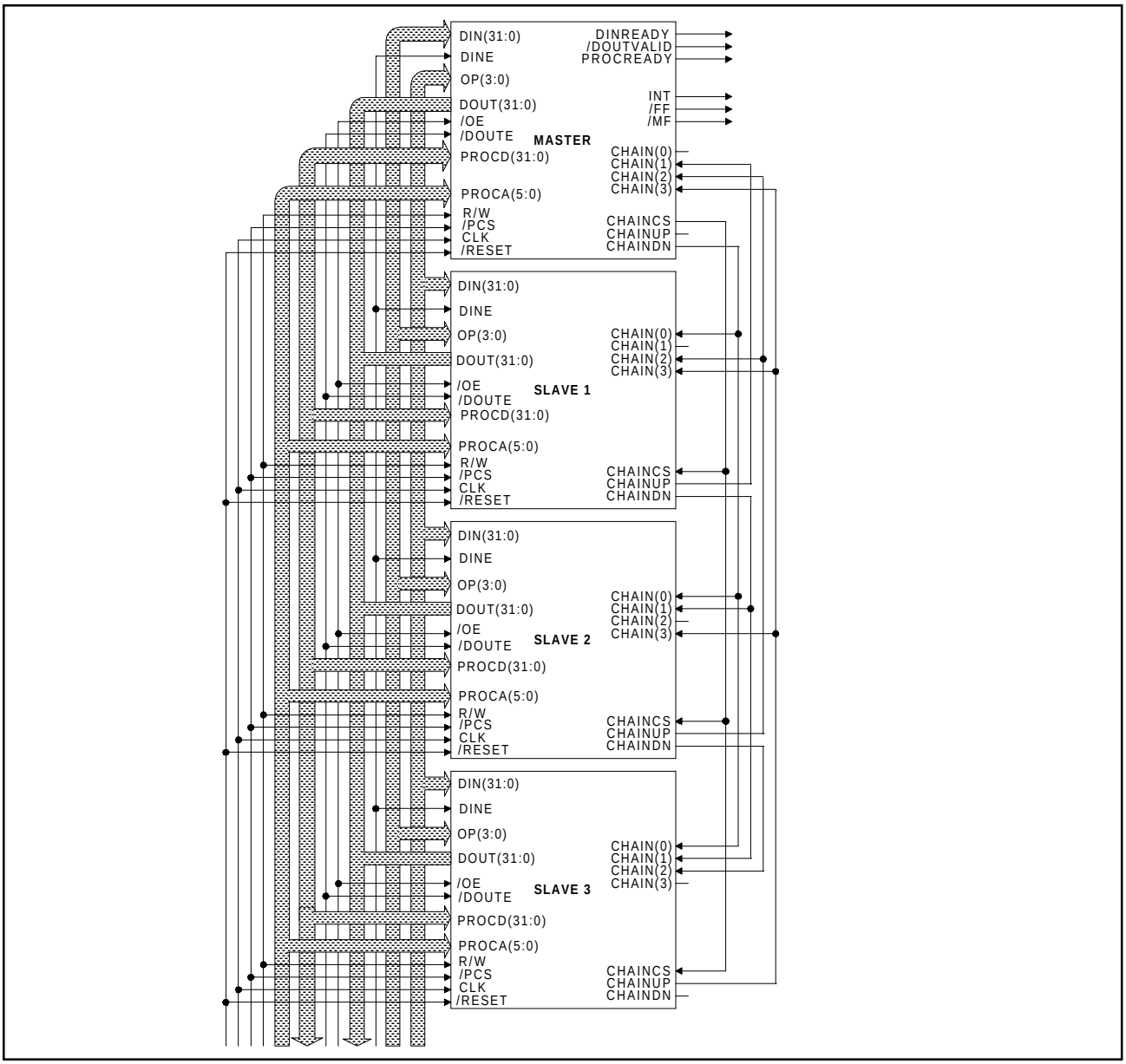

Figure 6: Four Devices Chained Together

DEVICE CHAINING

The MUAA CAM Family comes in 2K, 4K, and 8K deep devices. If an application requires a table that is larger than 8K, it is possible to transparently chain CAMs together. They are designed so that up to four CAMs can be connected together to provide a total memory depth of 32K without the need for any external logic. Figure 6 shows how four devices would be connected. Each CAM has a set of I/O pins that allow them to be connected in a chain. They are CHAIN(3:0), CHAINCS, CHAINUP, and CHAINDN. Only the CAM known as the MASTER provides the DINREADY, /DOUTVALID, PROCREADY, INT, /FF, and /MF outputs. They are left unconnected on the other CAMs. This scheme allows devices to be designed and included on the PCB but not fitted. The fit order would be MASTER, SLAVE1, SLAVE2, etc. The CAMs can be safely chained together with no need to worry about timing delays caused by internal flag ripple-through. Operation of a set of chained CAMs is identical to the operation of a single CAM whose size is equal to that of the chained devices. If the application required a table depth greater than 32K, external logic will be required to do parallel operations on each group of up to four CAMs.

CAM CODE

This section explains the code required when implementing an ARP cache using the MUAA CAM. It will show the data required and explain the timing of the relevant signals. Before the ARP cache can begin accepting ARP translation data, it must be configured to suit the application. Once configured, the MUAA CAM can be used to learn new translation data, add permanent translations, search for associated Ethernet addresses and delete individual entries. Although the configuration shown is for automatic aging, it is also possible to manually age out older entries. The registers that are required for configuration can only be accessed from the processor port. Therefore the configuration routine will be shown with reference to the signals required for processor port data transfer.

The other routines will be shown for access through both the processor port and the synchronous port. This will allow a system designer to implement an ARP cache accessible through the system processor bus or if required through some hardware control logic. The signal values shown for PROCA are shown for 32-bit mode. Therefore PROCA bit 0 must be held at a valid logic level. Please note that the signals specified in this section are shown without reference to appropriate timing considerations. The MUAA CAM Family data sheet contains all the relevant timing information for the signals required for both synchronous and processor port data transfer.

MUAA CAM Configuration

Table 4 shows the data that is required to configure the MUAA CAM in the following way:

- 32 bit I/O in both the synchronous and processor ports.
- 32 bits CAM and 48 bits RAM. This allows the IP addresses to be loaded in 1 clock cycle and the associated Ethernet addresses read out in 2 clock cycles.
- /DOUTVALID is on the same CLK signal as the data.
- INT is active HIGH
- LQUEUE, AQUEUE, PWEX, and SWEX interrupts are enabled.
- The auto-aging function is enabled.
- AQUEUE is enabled.
- The synchronous port is given higher priority than the processor port.
- The port address index will be available to be read from DOUT after the associated data.
- The auto-aging function will have the lowest priority during internal arbitration.
- The interval between automatic removal of older entries in the translation table is 0.5 seconds at 50MHz.
- The number of aging intervals before an entry is removed is 1800 (i.e., 15 minutes).

It should be noted that the AQUEUE and LQUEUE interrupts are enabled in this configuration only to show how this can be done. An ARP cache can function without

Line	/PCS	R/W	PROCA(5:1)	PROCD(31:0)	Description
1	L	L	10000b	00007F18h	Set up Configuration register
2	L	L	11000b	017D7840h	Sets Auto-age Interval register as 0.5 seconds at 50MHz
3	L	L	11001b	00000708h	Sets up the Learned Entry Life register as 1800 decimal (i.e., 15 minutes)

Table 4: CAM Cycle Sequence for Deleting an Entry

this facility as it is only required if upper level or management software wishes to keep track of learned or aged entries. The auto-age function is turned on and set to 708h (1800d) aging intervals per entry life with an interval of 0.5 second. These values were arbitrarily chosen in order to show how the CAM is configured. The actual values required would depend on how many different IP addresses the ARP cache is expected to store within a given time frame.

To configure the MUAA CAM, the three registers shown in Table 4 are loaded with the relevant data. The appropriate register is selected by loading the PROCA bus with the value associated with it. The data is applied to PROCD(31:0) while asserting /PCS and R/W LOW. The data will be accepted by the appropriate register at the rising edge of /PCS. The MUAA CAM will assert PROCREADY HIGH to indicate that the data has been accepted.

IP to Ethernet Translation

The translation is accomplished by loading the data port with the 32-bit IP address and monitoring the /MF flag or MF register. When using the synchronous port the hardware /MF pin will show if the was a MATCH. If the processor port is used, the MATCH result must be found by reading either the Address Index register of the MF flag register. If there is a match, /MF is asserted LOW (or MF register flag is set to 1) and the associated 48-bit Ethernet address can be read from the CAM in two cycles. Both port signal values are shown to allow a hardware or software solution to be implemented.

Table 5 shows the signals and data required when using the synchronous port for translation. This involves loading the synchronous port of the CAM with the destination IP address that requires address resolution. The 32-bit address is placed on DIN and the searcha <DIN> instruction is issued. The IP address is compared with the 32-bit CAM partition of the memory array. Searcha <DIN> is used in order to automatically update the age or time stamp of the entry when a MATCH is found. Alternatively, search <DIN> (Op-code 0011b) can be used if aging is not required.

The search operation takes four CLK periods after the instruction is given. The /DOUTVALID output will be asserted LOW for one CLK period when the results are available. If the search finds a MATCH, (/MF is asserted LOW) the associated Ethernet address can be read from DOUT in two cycles. When /DOUTVALID is detected being asserted LOW, bits <31:0> of the address can be read by asserting /OE. /DOUTE is asserted LOW to strobe the subsequent 32-bit words from DOUT. Line 3 shows bits <47:32> of the address being read from DOUT. Bits <31:16> of DOUT can be discarded at this point as they are unused in the data transfer. If the address index is required, it is read in line 4.

Synchronous port

Line	Mnemonic	/DINE	OP(3:0)	DIN(31:0)	Description	Notes
1	searcha<DIN>	L	0100b	DA bits <31:0>	Load DIN with the 32-bit IP address and initiate a search (with auto-aging).	

If /MF is asserted to indicate a MATCH and /DOUTVALID is asserted to indicate valid data, the following will read the associated Ethernet address (and address index if required):

Line	/OE	/DINE	/DOUTE	DOUT(31:0)	Description	Notes
2	L	H	H	Ethernet <31:0>	Read the associated data from MATCH location to find the corresponding Ethernet address.	1
3	L	H	L	Ethernet <47:32>	Read the remaining bits.	2
4	L	H	L	index <31:0>	Read the address index if required.	3

NOTES:

1. The MUAA CAM was configured during the configuration routine to place the associated data (RAM partition) onto the DOUT pins before the address index. This can be configured to allow the address index to be placed onto the pins first.
2. Bits <47:32> of the Ethernet address are placed on DOUT <15:0>. DOUT <31:16> bits should be discarded and not used during the data transfer. /DOUTE is asserted LOW to clock out the next word from the CAM.
3. /DOUTE is asserted LOW by the host system to clock out the next word from the CAM. In this case it is the address index of the matched location. If the address index is not required, line 4 can be ignored.

Table 5: Signal Values to Search CAM Using Synchronous Port

If the result of the search is a NO-MATCH condition, (/MF is held HIGH) the translation data is not held within the ARP cache. Therefore the upper-level software is unable to transmit its data and the ARP request and reply procedure must be carried out. An ARP request is sent and the subsequent reply is used to update the cache and provide the required destination hardware address to enable the upper level software to complete its data transfer.

Table 6 shows the signals and data required when using the processor port for translation. This involves loading the processor port of the CAM with the destination IP address that requires address resolution. The 32-bit address is placed on PROCD and the searcha <DIN> instruction is issued. The IP address is compared with the 32-bit CAM partition of the memory array. Searcha <DIN> is used in order to automatically update the age or time stamp of the entry when a MATCH is found. Alternatively, search <DIN> (register 00011b) can be used if aging is not required.

The search takes four CLK periods after the instruction is given. The PROCREADY output will be asserted HIGH when the results are available. At this point the /MF hardware output flag cannot be inspected to find the result of the comparison. Instead, the MF Flag register would be read to determine the result and is shown in line 2. If the result was a MATCH, the associated Ethernet address is read from the DOUT register in two cycles. When PROCREADY is detected being asserted HIGH, bits <31:0> of the address can be read by loading the PROCA bus with the DOUT register address and asserting /PCS LOW.

Line 4 shows bits <47:32> of the address being read from the DOUT register. Bits <31:16> can be discarded at this point as they are unused in the data transfer. If the address index is required, it is read from the Address Index register in line 5. During all data reads from the processor port, PROCREADY is used for flow control. The MUAA CAM will hold it LOW until the data in the appropriate register is valid.

Learn New Translation Data

New translation data has to be added to the MUAA CAM after the ARP request and reply process has been completed. To reduce the amount of ARP traffic, all the network packets that are received by a node can also be monitored. This will allow the NIC to constantly update the cache with new translation data gained from the incoming network packets. Once a new translation is found, the IP address and its corresponding Ethernet address are written into the CAM memory array and a new time stamp or age is automatically added. Both port signal values are shown to allow a hardware or software solution to be implemented.

Table 7 shows the signals and data required when using the synchronous port for adding new data. This involves loading the synchronous port of the CAM with the IP and

Processor port

Line	/PCS	R/W	PROCA(5:1)	PROCD(31:0)	Description	Notes
1	L	L	00100b	IP address	Write IP address to the searcha register	
2	L	H	10001b	MF flag (bit 1)	Read MF register to determine result of previous comparison. MF = 1 indicates a match.	1

If MF bit was equal to 1, the following will read the associated Ethernet address (and address index if required):

3	L	H	01101b	Ethernet address Bits <31:0>	Bits <31:0> of the Ethernet address are read from the DOUT register	2
4	L	H	01101b	Ethernet address Bits <47:32>	The remaining Ethernet bits are read from the DOUT register	3
5	L	H	10011b	Address index	Read the address index if required	4

NOTES:

1. The MF flag will be available on bit 1 of PROCD(31:0). The other bits can be discarded when reading this register.
2. The MUAA CAM was configured during the configuration routine to place the associated data (RAM partition) into the DOUT register before the address index. This can be configured to allow the address index to be placed into the register first.
3. Bits <47:32> of the Ethernet address are placed on bits <15:0> of the DOUT register. Bits <31:16> should be discarded and not used during the data transfer
4. The address index of the matched location is available in the Address Index register after the associated data. If the address index is not required, line 5 can be ignored.

Table 6: Signal Values to Search CAM Using Processor Port

Ethernet addresses in three cycles. The IP address is written to the CAM partition and the Ethernet address is written to the RAM partition. It is done in 3 steps: Line 1 loads the IP address. Line 2 loads bits <31:0> of the Ethernet address. Line 3 loads the remaining 16 bits of the Ethernet address on bits <15:0> of the DIN input and initiates the learn operation. The most significant bits on DIN at this point are discarded.

The learn operation causes the IP address to be compared with the CAM partition. If the comparison results in a NO-MATCH condition being given, the 80-bit translation data is added to the next free location of the memory array. At this point the most recent time-stamp or age is automatically added to the entry. If the result is a MATCH condition, the 48-bit Ethernet address and the time-stamp or age are updated. This is unlikely to occur because new translation data is only added after a search has already shown that the IP address is not located in the memory array.

Table 8 shows the signals and data required when using the processor port for adding new data. This involves loading PROCD with the IP and Ethernet addresses in three cycles. The IP address is written to the CAM partition and the Ethernet address is written to the RAM partition. It is done in 3 steps: Line 1 loads the IP address; Line 2 loads bits <31:0> of the Ethernet address; Line 3 loads the remaining 16 bits of the Ethernet address on bits <15:0> of PROCD and initiates the learn operation. The most significant bits on PROCD at this point are discarded. Once the 80-bit data word has been written to the CAM, it updates the entry in the same way as described for the synchronous port.

Add Permanent Entries

In certain circumstances the ARP request and reply process may not produce the translation information required. An example of this would be when a node does not have the capability to reply to ARP requests about its address information. If there is no proxy ARP on the network, the translation for the "dumb" node has to be added to the ARP cache manually. When it is added to the cache in this way, it must be marked as a permanent entry to ensure that it is not removed during the automatic aging process. The insert instruction is used to add the entry as a permanent one. The delete instruction can be used to remove the entry when it is no longer valid.

Synchronous port

Line	Mnemonic	/DINE	OP(3:0)	DIN(31:0)	Description	Notes
1	load<DIN>	L	0001b	IP address	Load DIN with the 32-bit IP address	
2	load<DIN>	L	0001b	Ethernet address bits <31:0>	Load DIN with first 32 bits of the Ethernet address	
3	learn<DIN>	L	0101b	Ethernet address bits <47:32>	Load DIN with the remaining 16 bits of the Ethernet address and add all 80 bits to CAM memory array (add time stamp)	1

NOTES:

1. Bits <47:32> of the Ethernet address are placed on DIN <15:0>. DIN <31:16> bits are discarded and not used during the load.

Table 7: Signal Values to Add New Translation Data Using the Synchronous Port

Processor port

Line	/PCS	R/W	PROCA(5:1)	PROCD(31:0)	Description	Notes
1	L	L	00001b	IP address	Load PROCD with the 32-bit IP address	
2	L	L	00001b	Ethernet address bits <31:0>	Load PROCD with first 32 bits of the Ethernet address	
3	L	L	00101b	Ethernet address bits <47:32>	Load PROCD with the remaining 16 bits of the Ethernet address and add all 80 bits to CAM memory array (add time stamp)	1

NOTES:

1. Bits <47:32> of the Ethernet address are placed on PROCD <15:0>. PROCD <31:16> bits are discarded and not used during the load.

Table 8: Signal Values to Add New Translation Data Using the Processor Port

Table 9 shows the signals and data required when using the synchronous port for adding permanent data. This involves loading the synchronous port of the CAM with the IP and Ethernet addresses in three cycles. The IP address is written to the CAM partition and the Ethernet address is written to the RAM partition. It is done in 3 steps: Line 1 loads the IP address; Line 2 loads bits <31:0> of the Ethernet address; Line 3 loads the remaining 16 bits of the Ethernet address on bits <15:0> of the DIN input and initiates the insert operation. The most significant bits on DIN at this point are discarded.

The insert operation causes the IP address to be compared with the CAM partition. If the comparison results in a NO-MATCH condition being given, the 80-bit translation data is added to the next free location of the memory array. If the result is a MATCH condition, the 48-bit Ethernet address is over-written into the RAM partition of the matching location. In both cases, the entry is marked as a permanent one and will not be removed by the automatic-aging function.

Table 10 shows the signals and data required when using the processor port for adding permanent data. This involves loading PROCD with the IP and Ethernet addresses in three cycles. The IP address is written to the CAM partition and the Ethernet address is written to the RAM partition. It is done in 3 steps: Line 1 loads the IP address; Line 2 loads bits <31:0> of the Ethernet address; Line 3 loads the remaining 16 bits of the Ethernet address on bits <15:0> of PROCD and initiates the insert operation. The most significant bits on PROCD at this point are discarded. Once the 80-bit data word has been written to the CAM, it updates the entry in the same way as described for the synchronous port.

Delete Individual Translation Data Entries

Translation data can be removed from the MUAA CAM if it is found to be incorrect or out of date. Both port signal values are shown to allow a hardware or software solution to be implemented. Table 11 shows the signals and data required when using the synchronous port for deleting data. This involves loading the synchronous port of the CAM with the IP address of the data to be removed. The IP address is written to the CAM partition while loading OP(3:0) with the instruction required to delete an entry. The IP address will be compared with the CAM partition of the memory array and deleted when it is found. The MUAA will assert / MF LOW to indicate that the comparison produced a MATCH and the matching location was deleted. The address index is made available at DOUT to enable any further associated data to also be removed. /DOUTVALID will be asserted LOW for one CLK period by the MUAA CAM to indicate the presence of a valid address index is at DOUT.

Table 12 shows the signals and data required when using the processor port for deleting data. This involves loading PROCD with the IP address that has to be removed. The IP address is written to the CAM partition while loading PROCA(5:1) with the value of the register required to delete an entry. The IP address will be compared with the CAM partition of the memory array and deleted when it is found. The address index is made available in the Address Index register along with the result of the comparison. The MUAA CAM, to indicate that the comparison results are available, asserts PROCREADY HIGH. Line 2 shows how the Address Index register is read to give the comparison result and the address index of the deleted entry. Bits <25:0> will indicate the address index and bit 30 will indicate the result. Bit 30 will be equal to 1 if the result was a NO-MATCH condition and it will be equal to 0 if it was a MATCH. If the address index is not required, reading the Address Index register when PROCREADY is asserted will still indicate that the translation data was successfully deleted. Reading the MF flag register (PROCA(5:1) =1001b) can also do this.

Synchronous port

Line	Mnemonic	/DINE	OP(3:0)	DIN(31:0)	Description	Notes
1	load<DIN>	L	0001b	IP address	Load DIN with the 32-bit IP address	
2	load<DIN>	L	0001b	Ethernet address bits <31:0>	Load DIN with first 32 bits of the Ethernet address	
3	insert<DIN>	L	0010b	Ethernet address bits <47:32>	Load DIN with the remaining 16 bits of the Ethernet address and add all 80 bits to CAM memory array (and mark as permanent)	1

NOTES:

1. Bits <47:32> of the Ethernet address are placed on DIN <15:0>. DIN <31:16> bits are discarded and not used during the load.

Table 9: Signal Values to Add Permanent Translation Data Using the Synchronous Port

Aging out Older Entries Manually

The MUAA CAM can automatically age out older entries when the auto-age function is selected. Whether this option is configured or not, the user has full control over the purging of older entries. Manual aging can be performed if auto-aging is not configured or extra purges can be initiated if for example the /FF hardware flag indicates that the device is full. Either port can be used to manually age out the entries. Table 13 shows the signal values required when removing older entries from the CAM using the synchronous port. When the command is given, all non-permanent entries are compared with the age counter. The resulting MATCH locations are deleted (or added to the AQUEUE if it is enabled) and therefore aged out or purged.

Table 14 shows the signal values required when removing older entries from the CAM using the processor port. /PCS is asserted LOW to indicate a processor port cycle and R/W is asserted LOW to indicate a write cycle. The MUAA CAM will assert PROCREADY HIGH to indicate that the data has been accepted.

Processor port

Line	/PCS	R/W	PROCA(5:1)	PROCD(31:0)	Description	Notes
1	L	L	00001b	IP address	Load PROCD with the 32-bit IP address	
2	L	L	00001b	Ethernet address bits <31:0>	Load PROCD with first 32 bits of the Ethernet address	
3	L	L	00010b	Ethernet address bits <47:32>	Load PROCD with the remaining 16 bits of the Ethernet address and add all 80 bits to CAM memory array (mark as permanent)	1

NOTES:

1. Bits <47:32> of the Ethernet address are placed on PROCD <15:0>. PROCD <31:16> bits are discarded and not used during the load.

Table 10: Signal Values to Add Permanent Translation Data Using the Processor Port

Synchronous port

Line	Mnemonic	/DINE	OP(3:0)	DIN(31:0)	Description	Notes
1	delete<DIN>	L	0110b	IP address	Load DIN with the 32-bit IP address and initiate a delete operation	

If /MF is asserted to indicate a MATCH and /DOUTVALID is asserted to indicate valid data, the following will read the address index if required:

Line	/OE	/DINE	/DOUTE	DOUT(31:0)	Description	Notes
2	L	H	H	Address index bits <31:0>	Read the address index of the deleted entry	1

NOTES:

1. The address index of the matched location is available at DOUT after the deletion has been performed. If the address index is not required, line 2 can be ignored.

Table 11: Signal Values to Delete Translation Data Using the Synchronous Port

Processor port

Line	/PCS	R/W	PROCA(5:1)	PROCD(31:0)	Description
1	L	L	00110b	IP address	Load PROCD with the 32-bit IP address and initiate a delete operation

When PROCREADY is asserted HIGH to indicate that the internal comparison (and deletion if possible) is complete, the result and Address index can be read:

2	L	H	10011b	Address index bits <25:0> /MF bit 30	Read the address index of the deleted entry and the comparison result from the Address Index register

Table 12: Signal Values to Delete Translation Data Using the Processor Port

Synchronous port

Line	Mnemonic	/DINE	OP(3:0)	DIN(31:0)	Description	Notes
1	age	L	0111b	xxxxxxxxh	Age out older entries	1

NOTES:

xxxxxxxxh = Don't care.

Table 13: Signal Values to Purge Older Entries Using the Synchronous Port

Processor port

Line	/PCS	R/W	PROCA(5:1)	PROCD(31:0)	Description	Notes
1	L	L	00111b	xxxxxxxxh	Age out older entries	1

Notes:

xxxxxxxxh = Don't care.

Table 14: Signal Values to Purge Older Entries Using the Processor Port

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