16-BIT LANCAM® ROUTINES FOR AN 8-PORT 100BASE-T ETHERNET SWITCH

INTRODUCTION

This application note focuses on how to control MUSIC's MU9Cx480A-Series LANCAM family to support an 8-port 100Base-T Ethernet bridge or switch. The routine timing is based on a 50MHz state machine controlling 70ns speed grade CAMs. Arbitration between the ports is beyond the scope of this document, since that gets into system architecture. This document outlines the initialization and configuration of the CAM database, the Destination and Source Address filtering routines, address learning, aging and purging of entries, and other table and system management routines.

All routines in this document are written as non-interruptible routines. This means a routine that is running must complete before another routine is allowed to start. While this approach may be tougher on the system arbiter, it keeps the routines short and execution fast.

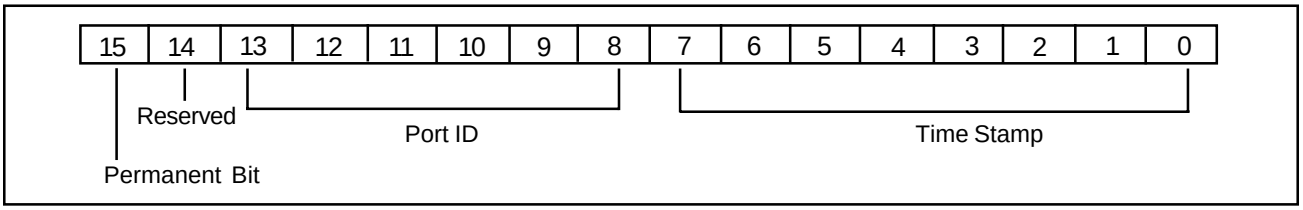
INITIALIZATION AND CONFIGURATION OF THE CAM DATABASE

The Initialization and Configuration Routine configures four MU9Cx480A-series LANCAMs for use with the following filter and table management routines (note that the indicated /E = H timing will support a daisy chain of up to five 70ns LANCAMs. Lines 1 through 18 initialize the LANCAMs. Line 1 clears up any power-up anomalies that may be left in the part. Lines 2 and 3 set all devices to listen to the following commands. Lines 4 and 5 reset the devices.

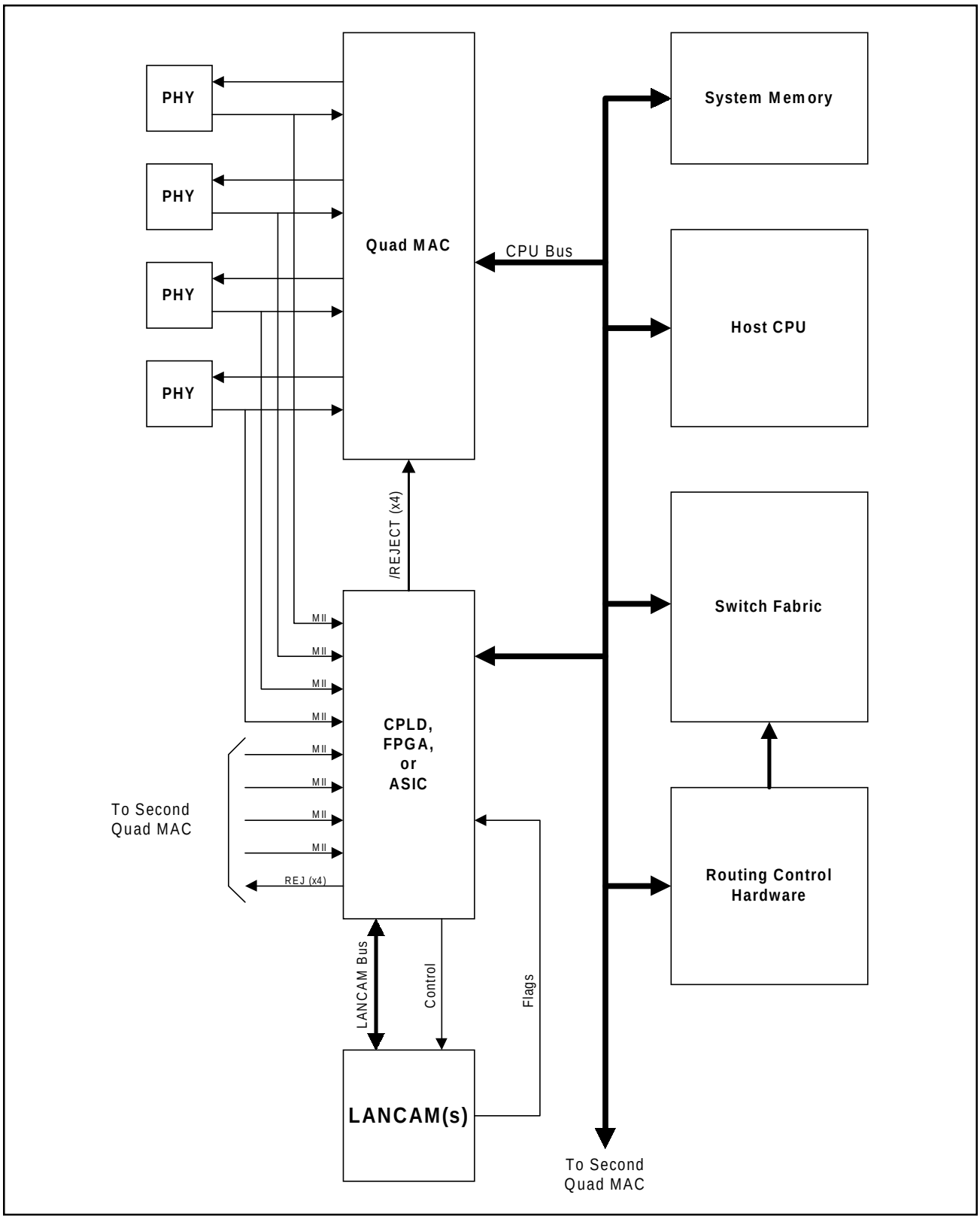
Lines 6 through 18 give a unique Page address to each CAM in the chain. Line 6 targets the Page Address register of the highest-priority (lowest address value) device in the chain. Line 7 sets the Page Address value. Line 8 sets the Full flag on this device, forcing the next device in the chain to respond to the next set of initialization commands. This cycle of targeting the Page Address register, setting the Page Address value, and setting the Full Flag is repeated until all devices in the chain have a unique Page Address value. Lines 17 and 18 reset all devices, returning the Full flags to their normal function.

Lines 19 through 30 configure the Background Register set for use in the Purge on Time Stamp, Set Address register, and Read Entries routines. Lines 20 and 21 configure the CAMs as 64 bits CAM, 0 bits RAM, and use Mask Register 1 for compares. Lines 22 to 26 initialize Mask Register 1, for use in comparing on only the Time Stamp and Permanent bits. Lines 27 and 28 set the Segment Control register to write to Segment 0 (Permanent bit, Port ID, Time Stamp), and read from Segments 0 through 3. Line 29 sets the Persistent destination for Data writes to the Comparand register. Line 30 sets the Persistent source for Data reads to memory at Address register (the memory location to which the Address register is pointing).

Lines 31 through 42 configure the Foreground Register set for the DA and SA filtering operations, and the addition and deletion of permanent entries. Lines 32 and 33 configure the CAMs as 48 bits CAM, 16 bits RAM, and invoke no mask registers for compares. Lines 34 and 35 set the Segment Control register to write to Segments 0 to 3, and read from Segment 0. Lines 36 to 40 initialize Mask Register 1, which is used during the update operation of the SA Filter routine. Line 41 sets the Persistent destination to the Comparand register, and Line 42 sets the Persistent source to the Highest Match (highest-priority matching memory location's Associated data).



Associated Data Field Bit Assignments



Typical Switch Block Diagram

The CAM database has been configured to have Segment 0 (16-bit segment) contain the Associated Data field, which is the Time Stamp, Port ID, and Permanent bit. The remaining 3 segments contain the 48-bit Ethernet address. The Mask registers in both the Foreground Register set and Background Register set have been configured to have the following Associated Data Field bit assignments: 8 bits of Time Stamp to support a resolution of 1-of-256, 6 bits of Port ID to support up to 64 ports, and the Permanent bit feature to support addresses that do not get aged out. These bit assignments are shown in the table on page 1.

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	L	H	20	20	H		XXXXH	Command read-Clears Power-up anomalies
2	L	L	20	20	H	TCO_DS	0228H	Target Device Select register
3	L	L	20	20	H		FFFFH	Select all devices
4	L	L	20	20	H	TCO_CT	0200H	Target Control register
5	L	L	40	20	H		0000H	Reset all devices
6	L	L	20	20	H	TCO_PA	0208H	Target Page Address register
7	L	L	20	20	H		0000H	Set Page Address = 0 for 1st device
8	L	L	60	20	H	SFF	0700H	Set Full flag
9	L	L	20	20	H	TCO_PA	0208H	Target Page Address register
10	L	L	20	20	H		0001H	Set Page Address = 1 for 2nd device
11	L	L	60	20	H	SFF	0700H	Set Full flag
12	L	L	20	20	H	TCO_PA	0208H	Target Page Address register
13	L	L	20	20	H		0002H	Set Page Address = 2 for 3rd device
14	L	L	60	20	H	SFF	0700H	Set Full flag
15	L	L	20	20	H	TCO_PA	0208H	Target Page Address register
16	L	L	20	20	H		0003H	Set Page Address = 3 for 4th device
17	L	L	20	20	H	TCO_CT	0200H	Target Control register
18	L	L	40	20	H		0000H	Resets Full flag in all devices
19	L	L	20	20	H	SBR	0619H	Select Background Register set
20	L	L	20	20	H	TCO_CT	0200H	Target Control register
21	L	L	20	20	H		8011H	64 CAM,0 RAM,MR1,2480 Enhanced Mode,Incr AR
22	L	L	20	20	H	SPD_MR1	0108H	Set Persistent destination to MR1
23	H	L	20	20	H		7F00H	Segment 0: Time Stamp and Perm bit only
24	H	L	20	20	H		FFFFH	Segment 1
25	H	L	20	20	H		FFFFH	Segment 2
26	H	L	20	20	H		FFFFH	Segment 3
27	L	L	20	20	H	TCO_SC	0210H	Target Segment Control register
28	L	L	20	20	H		00C0H	Write Segment 0, Read Segments 0:3
29	L	L	20	20	H	SPD_CR	0100H	Set Persistent destination to Comparand
30	L	L	20	20	H	SPS_M@[AR]	0004H	Set Persistent source to Memory @ AR
31	L	L	20	20	H	SFR	0618H	Select Foreground Register set
32	L	L	20	20	H	TCO_CT	0200H	Set Control register
33	L	L	20	20	H		8041H	48 CAM,16 RAM,No Mask,2480 Enhanced Mode,Incr AR
34	L	L	20	20	H	TCO_SC	0210H	Set Segment Control register
35	L	L	20	20	H		1800H	Write Segments 0:3, Read Segment 0
36	L	L	20	20	H	SPD_MR1	0108H	Set Persistent destination to MR1
37	H	L	20	20	H		8000H	Segment 0: Mask Perm bit only
38	H	L	20	20	H		0000H	Segment 1
39	H	L	20	20	H		0000H	Segment 2
40	H	L	20	20	H		0000H	Segment 3
41	L	L	20	20	H	SPD_CR	0100H	Set Persistent destination to Comparand
42	L	L	20	20	H	SPS_HM	0005H	Set Persistent source to Highest Match

Initialization and Configuration Routine

NOTES:

1. xxxx = Don't Care
2. dddd = Data Value written to or read from the CAM database
3. aaaa = Address of the CAM Memory location to be read
4. pppp = Page Address value of the device to be read

ADDRESS FILTER ROUTINES

The Destination Address Filter routine is the highest-priority routine, followed closely by the Source Address Filter routine. Each of these routines may need to be run up to eight times per arbitration cycle (once for each of eight ports), which implies that under the worst case condition of all eight ports receiving a packet at the same time, the associated data from the DA filter routine will be available for the last port after 2.4 µs. One of the management routines can be run once per arbitration cycle, since these routines are far less time critical.

The Match flag is available by the end of the data cycle on Line 4. The Associated data is read to get the Port ID of the matching entry. If the Port ID is the same as the port initiating the DA routine, the port should be signaled to reject the frame (assuming negative filtering).

Note that the SA Filter routine requires a decision to be made in the state machine, based on whether or not a match exists. If a match is found, line 5a updates the Time Stamp and Port ID are updated by moving the contents of the Comparand register through MR1 to the location of the highest priority match in the CAM. If a match is not found, line 5b learns the new address is learned, along with its Port ID and the current Time Stamp, by moving the contents of the Comparand register to the Next Free memory location. Also note that the Permanent bit is always 0, ensuring that any Source addresses learned by this routine can be purged if they become inactive.

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	H	L	20	20	H		xxxxH	Dummy write to Segment 0
2	H	L	20	20	H		ddddH	Write 1st 16 bits to Segment 1
3	H	L	20	20	H		ddddH	Write 2nd 16 bits to Segment 2
4	H	L	60	40	L		ddddH	Write 3rd 16 bits to Segment 3 and compare
5	H	H	60	20	H		ddddH	Read Associated data, FFFFH if no match

DA Filter Routine - Total Time=300ns

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	H	L	20	20	H		ddddH	Write Perm bit = 0, Port ID and TS to Segment 0
2	H	L	20	20	H		ddddH	Write 1st 16 bits to Segment 1
3	H	L	20	20	H		ddddH	Write 2nd 16 bits to Segment 2
4	H	L	60	40	L		ddddH	Write 3rd 16 bits to Segment 3 and compare

If a match is found, Update Time Stamp and Port ID

5	L	L	60	20	H	MOV_HM, CR, MR1	0368H	Move to Highest Match through MR1 to update Time Stamp and Port ID

If no match is found, Learn new address

5	L	L	60	20	H	MOV_NF,CR,V	0334H	Moves SA to Next Free w/ Time Stamp and Port ID

SA Filter Routine - Total Time=300ns

TABLE MANAGEMENT ROUTINES

The following table management routines are low-priority routines. One of these routines may be run per arbitration cycle, with the Purge on Time Stamp routine being the highest-priority management routine. Adding a permanent entry, deleting an entry, or reading the contents of the CAM database are not time critical. The system performance will not be impacted if these routines are held off for a few arbitration cycles.

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	L	L	20	20	H	SBR	0619H	Select Background Register set
2	H	L	60	20	H		ddddH	Purge Time Stamp value and compare
3	L	L	60	20	H	VBC_ALM,E	043DH	Mark all matching entries “Empty”
4	L	L	20	20	H	SFR	0618H	Select Foreground Register set

Purge on Time Stamp - Total Time=240ns

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	H	L	20	20	H		ddddH	Write Perm bit and Port ID to Segment 0
2	H	L	20	20	H		ddddH	Write 1st 16 bits to Segment 1
3	H	L	20	20	H		ddddH	Write 2nd 16 bits to Segment 2
4	H	L	20	20	H		ddddH	Write 3rd 16 bits to segment 3
5	L	L	60	20	H	MOV_NF,CR,V	0334H	Move to Next Free

Add a Permanent Entry - Total Time=240ns

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	H	L	20	20	H		xxxxH	Dummy write to Segment 0
2	H	L	20	20	H		ddddH	Write 1st 16 bits to Segment 1
3	H	L	20	20	H		ddddH	Write 2nd 16 bits to Segment 2
4	H	L	60	40	L		ddddH	Write 3rd 16 bits to Segment 3 & compare
5	L	L	60	20	H	VBC_HM,E	042DH	Set Highest Match to “Empty”

Delete an Entry - Total Time=300ns

SYSTEM SUPERVISORY ROUTINES

These routines are included to aid the system in keeping track of the active addresses in the system, such as a shadow table stored in system memory. The Set Address Register routine needs only to be run once to initialize the Address register for a group of reads. Each read of the CAM will increment the Address register automatically, so the next read will access the next address in the CAM. The Page address needs to be set each time the Read Entries routine is run.

The Read Entry routine must be repeated for each address in each device. Because the associative memory locations of Next Free, Highest Matching, and All Matching are used to add and delete entries from the CAM, not all locations will contain valid data. The Status register contains the validity status of the CAM location that was just read, so Status Register bits 29 and 28 must be checked. These bits will both be LOW for a Valid location.

TIMING ANALYSIS

In the worst-case scenario, we would like to have 8 DA Routines, 8 SA Routines, 1 Management routine and 1 Read Entry routine per arbitration cycle, completed within one minimum length frame of 6.2 µs for 100 Base-T. The worst-case timing for the routines shown here is 5.78 µs, which gives the arbiter 21 clock cycles to play with.

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	L	L	20	20	H	SBR	0619H	Select Background Register set
2	L	L	20	20	H	TCO_AR	0220H	Target Address register
3	L	L	20	20	H		aaaaH	Address value
4	L	L	20	20	H	SFR	0618H	Select Foreground Register set

Set Address Register - Total Time=60ns

Line	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0]	Description
1	L	L	20	20	H	SBR	0619H	Select Background Register set
2	L	L	20	20	H	TCO_DS	0228H	Target Device Select register
3	L	L	20	20	H		ppppH	Page Address value
4	H	H	60	20	H		ddddH	Data Read, Segment 0
5	H	H	60	20	H		ddddH	Data Read, Segment 1
6	H	H	60	20	H		ddddH	Data Read, Segment 2
7	H	H	60	20	H		ddddH	Data Read, Segment 3
8	L	H	40	20	H		ddddH	Command Read, Status Register bits 15:0
9	L	H	40	20	H		ddddH	Command Read, Status Register bits 31:16
10	L	L	20	20	H	TCO_DS	0228H	Target Device Select register
11	L	L	20	20	H		FFFFH	Select all devices
12	L	L	20	20	H	SFR	0618H	Select Foreground Register set

Read Entry - Total Time=680ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[15–0] (HEX)	Description
1								
2								
3								
4								
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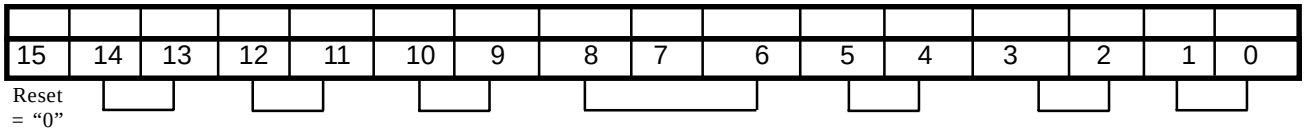
Blank Routine Worksheet



Match Flag
Enable = "00"
Disable = "01"
No Change="11"

Full Flag
Enable = "00"
Disable = "01"
No Change="11"

Translation
No Trans = "00"
Translated = "01"
No Change= "11"

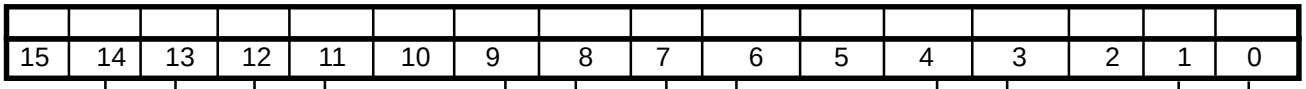
64 CAM / 0 RAM = "000"
48 CAM / 16 RAM = "001"
32 CAM / 32 RAM = "010"
16 CAM / 48 RAM = "011"
48 RAM / 16 CAM = "100"
32 RAM / 32 CAM = "101"
16 RAM / 48 CAM = "110"
No Change = "111"

Compare Mask
None = "00"
MR1 = "01"
MR2 = "10"
No Change= "11"

Address Register
Increment = "00"
Decrement = "01"
Disable = "10"
No Change = "11"

Mode
1480 = "00"
2480 = "01"
Reserved = "10"
No Change = "11"

Control Register Bit Assignments



Set Dest Segment Limits = "0" No Chng = "1"

Destination Count Start Limit "00 - 11"

Destination Count End Limit "00 - 11"

Set Source Segment Limits = "0" No Chng = "1"

Source Count Start Limit "00 - 11"

Source Count End Limit "00 - 11"

Load Destination Segment Count = "0" No Chng = "1"

Destination Segment Count Value "00 - 11"

Load Source Segment Count = "0" No Chng = "1"

Source Segment Count Value "00 - 11"

Segment Control Register Bit Assignments

NOTES

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