MUSIC SEMICONDUCTORS

Application Note AN-N17

32-BIT LANCAM® ROUTINES FOR A 12-PORT 100BASE-T ETHERNET SWITCH

INTRODUCTION

This application note focuses on how to control MUSIC's MU9Cx485A Series WidePort LANCAM family to support a 12-port 100Base-T Ethernet bridge or switch. The routine timing is based on a 50MHz state machine controlling 70ns speed grade CAMs. Arbitration between the ports is beyond the scope of this document, since that discussion gets into system architecture. This document outlines the initialization and configuration of the CAM database, the Destination and Source Address Filtering routines, address learning, aging and purging of entries, and other table and system management routines.

All routines in this document are written as non-interruptible routines. This means a routine that is running must complete before another routine is allowed to start. While this approach may be tougher on the system arbiter, it keeps the routines short and execution fast.

INITIALIZATION AND CONFIGURATION OF THE CAM DATABASE

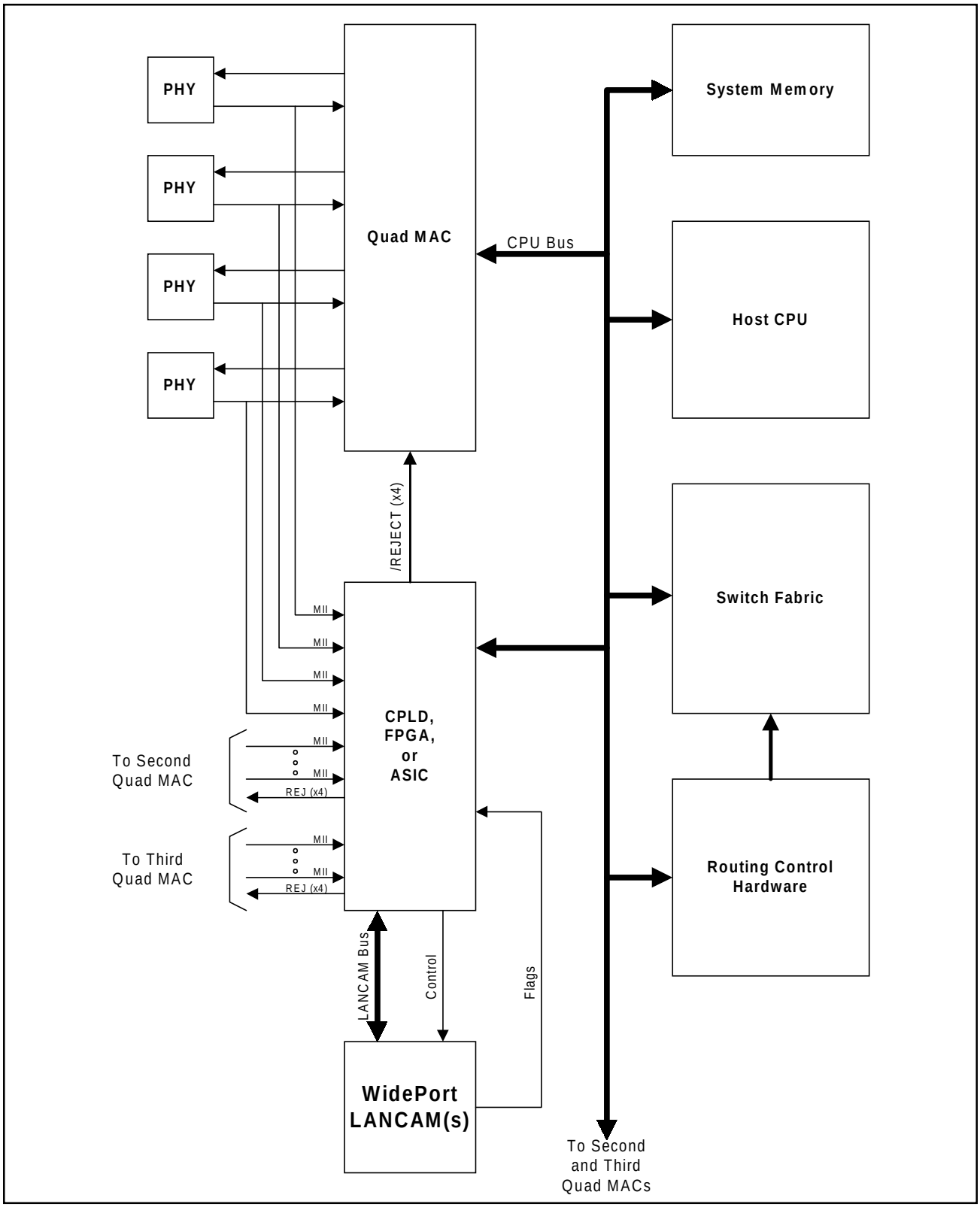
The Initialization and Configuration routine is constructed to configure four MU9Cx485A series WidePort LANCAMs for use with the following filter and table management routines (note that the indicated /E = H timings will support up to five 70ns devices). Lines 1 through 11 initialize the LANCAMs. Line 1 clears up any power-up anomalies that may be left in the part. Line 2 sets all devices to listen to the following commands. Line 3 resets the devices.

Lines 4 through 10 give a unique Page address to each CAM in the chain. Line 4 targets the Page Address register of the highest-priority (lowest address value) device in the chain and sets the Page Address value. Line 5 sets the Full flag on this device, forcing the next device in the chain to respond to the next set of initialization commands. This cycle of targeting the Page Address register, setting the Page Address value, and setting the Full flag is repeated until all devices in the chain have a unique Page Address value. Line 11 resets all devices, returning the Full flags to their normal function.

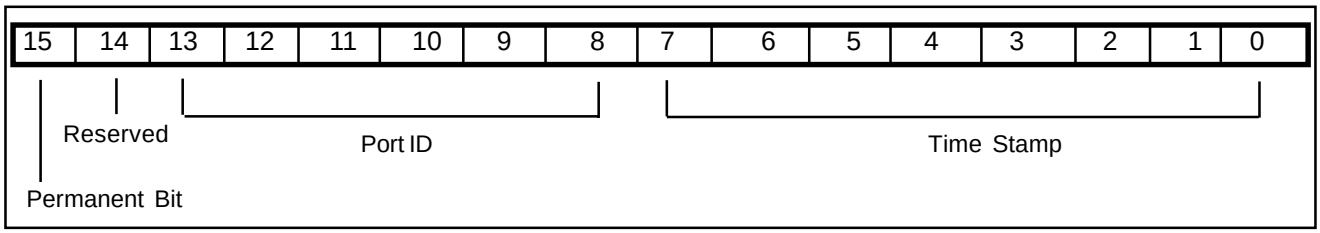
Lines 12 through 19 configure the Background Register set for use in the Purge on Time Stamp, Set Address Register, and Read Entries routines. Line 13 configures the CAMs as 64 bits CAM, 0 bits RAM, and Mask Register 1 for compares. The Address register is configured to auto-increment. Lines 14 to 16 initialize Mask Register 1 for use in comparing on only the Time Stamp and Permanent bits. Line 17 sets the Segment Control register to write to Segment 0 (Permanent bit, Port ID, Time Stamp), and read Segments 0 and 1. Line 18 sets the Persistent destination for Data writes to the Comparand register. Line 19 sets the Persistent source for Data reads to Memory at Address register (the memory location the Address register is pointing to).

Lines 20 through 27 configure the Foreground Register set for the DA and SA filtering operations, and the addition and deletion of permanent entries. Line 21 configures the CAMs as 48 bits CAM, 16 bits RAM, no mask register for compares, and sets the response mode to 2480. Line 22 sets the Segment Control register to write to Segments 0 to 1, and read from Segment 0. Lines 23 to 25 initialize Mask Register 1, which is used during the update operation of the SA Filter routine. Line 26 sets the Persistent destination to the Comparand register, and Line 27 sets the Persistent source to the Highest Match (highest-priority matching memory location's Associated data).

The CAM database has been configured to have the lowest 16 bits of the 64-bit entry contain the Associated Data field, which is the Time Stamp, Port ID, and Permanent bit. The remaining bits (bits 63–16) contain the 48-bit Ethernet address. The mask registers in both the Foreground Register set and Background Register set have been configured to have the following Associated Data Field bit assignments: 8 bits of Time Stamp to support a resolution of 1-of-256, 6 bits of Port ID to support up to 64 ports, and the Permanent Bit feature to support addresses that do not get aged out. These bit assignments are shown in the table on page 3.



Typical Switch Block Diagram



Associated Data Field (Lowest 16 bits) Bit Assignments

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	L	H	20	20	H		0000 0000	Command Read Clears Power-up anomalies
2	L	L	20	20	H	TCOW_DS	0A28 FFFF	Target Device Select register Select all devices
3	L	L	40	20	H	TCOW_CT	0A00 0000	Target Control register Reset all devices
4	L	L	20	20	H	TCOW_PA	0A08 0000	Target Page Address register Set Page address = 0 for 1st device
5	L	L	60	20	H	SFF	0700 0000	Set Full flag
6	L	L	20	20	H	TCOW_PA	0A08 0001	Target Page Address register Set Page address = 1 for 2nd device
7	L	L	60	20	H	SFF	0700 0000	Set Full flag
8	L	L	20	20	H	TCOW_PA	0A08 0002	Target Page Address register Set Page address = 2 for 3rd device
9	L	L	60	20	H	SFF	0700 0000	Set Full flag
10	L	L	20	20	H	TCOW_PA	0A08 0003	Target Page Address register Set Page address = 3 for 4th device
11	L	L	40	20	H	TCOW_CT	0A00 0000	Target Control register Resets Full flag in all devices
12	L	L	20	20	H	SBR	0619 0000	Select Background Register set
13	L	L	20	20	H	TCOW_CT	0A00 8011	Target Control register 64 CAM,0 RAM,MR1,2480 Mode,Incr AR
14	L	L	20	20	H	SPD_MR1	0108 0000	Set Persistent destination to MR1
15	H	L	20	20	H		FFFF 7F00	Bits 31–16 : Opaque mask Bits 15–0 : Time Stamp and Perm bit only
16	H	L	20	20	H		FFFF FFFF	Bits 31–0 : Opaque mask
17	L	L	20	20	H	TCOW_SC	0A10 0040	Target Segment Control register Write segment 0, Read segments 0:1
18	L	L	20	20	H	SPD_CR	0100 0000	Set Persistent destination to Comparand
19	L	L	20	20	H	SPS_M@[AR]	0004 0000	Set Persistent source to Memory @ AR
20	L	L	20	20	H	SFR	0618 0000	Select Foreground Register set
21	L	L	20	20	H	TCOW_CT	0A00 8041	Set Control register 48 CAM,16 RAM,No Mask,2480M,Incr AR
22	L	L	20	20	H	TCOW_SC	0A10 0800	Set Segment Control register Write Segments 0:1, Read Segment 0
23	L	L	20	20	H	SPD_MR1	0108 0000	Set Persistent destination to MR1
24	H	L	20	20	H		0000 8000	Bits 31–16 : Transparent mask Bits 15–0 : Mask Permanent bit only
25	H	L	20	20	H		0000 0000	Bits 31–0 : Transparent mask
26	L	L	20	20	H	SPD_CR	0100 0000	Set Persistent destination to Comparand
27	L	L	20	20	H	SPS_M@HM	0005 0000	Set Persistent source to Highest match

Initialization and Configuration Routine

NOTES:

1. xxxx = Don't Care
2. dddd = Data Value written to or read from the CAM database
3. aaaa = Memory location of CAM you want to read from
4. pppp = Page Address value of the device to be read from

ADDRESS FILTER ROUTINES

The Destination Address Filter routine is the highest-priority routine, followed closely by the Source Address Filter routine. Each of these routines may need to be run up to 12 times per arbitration cycle (once for each of 12 ports), which implies that under the worst-case conditions of all 12 ports receiving a minimum size packet at the same time, the associated data from the DA filter routine will be available for the last port after 2.64µs. One of the management routines can be run once per arbitration cycle, since these routines are far less time critical.

The Match flag is available by the end of the data cycle on Line 2. The associated data is read to get the Port ID of the matching entry. If the Port ID is the same as the port initiating the DA Routine, the port should be signaled to reject the frame (assuming negative filtering).

Note that the SA Filter Routine requires a decision to be made in the state machine, based on whether or not a match exists. If a match is found, line 3a updates the Time Stamp and Port ID are updated by moving the contents of the Comparand Register through MR1 to the location of the highest priority match in the CAM. If a match is not found, line 3b learns the new address, along with its Port ID and the current Time Stamp by moving the contents of the Comparand register to the Next Free memory location. Also note that the Permanent bit is always "0," ensuring that any Source Address learned by this routine can be purged if it becomes inactive.

TABLE MANAGEMENT ROUTINES

The following table management routines are low priority routines. One of these routines may be run per arbitration cycle, with the Purge on Time Stamp routine being the highest-priority management routine. Adding a permanent entry, deleting an entry, or reading the contents of the CAM database are not time critical. The system performance will not be impacted if these routines are held off for a few arbitration cycles.

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	H	L	20	20	H		dddd xxxx	Write lowest 16 bits of addr. to bits 31–16 Dummy write to bits 15–0
2	H	L	60	40	L		dddd dddd	Write highest 32 bits of addr. to bits 31–0 and compare
3	H	H	60	20	H		xxxx ddxx	Read Associated data, Port ID on bits 13–8 FFFF FFFF on bits 31–0 if no match

DA Filter Routine - Total Time=220ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	H	L	20	20	H		dddd dddd	Write lowest 16 of addr. bits to bits 31–16 Write Perm Bit, Port ID and TS to bits 15–0
2	H	L	60	40	L		dddd dddd	Write highest 32 bits of addr. to bits 31–0 and compare

If a match is found, Update Time Stamp & Port ID

3a	L	L	60	20	H	MOV_HM, CR, MR1	0368 0000	Move to Highest Match through MR1 to Update Time Stamp and Port ID

If no match is found, Learn new address

3b	L	L	60	20	H	MOV_NF, CR,V	0334 0000	Moves SA to Next Free w/ Time Stamp and Port ID

SA Filter Routine - Total Time=220ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	L	L	20	20	H	SBR	0619 0000	Select Background Register set
2	H	L	60	20	H		xxxx 00dd	Load Time Stamp value to purge and compare
3	L	L	60	20	H	VBC_ALM,E	043D 0000	Mark all matching entries “Empty”
4	L	L	20	20	H	SFR	0618 0000	Select Foreground Register set

Purge on Time Stamp - Total Time=240ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	H	L	20	20	H		dddd ddxx	Write lowest 16 bits of addr. to bits 31–16 Write Perm Bit and Port ID to bits 15–8
2	H	L	20	20	H		dddd dddd	Write highest 32 bits of addr. to bits 31–0
3	L	L	60	20	H	MOV_NF, CR,V	0334 0000	Move to Next Free

Add a Permanent Entry - Total Time=160ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0]	Description
1	H	L	20	20	H		dddd xxxx	Write lowest 16 bits of addr. to bits 31–16 Dummy Write to bits 15–0
2	H	L	60	40	L		dddd dddd	Write highest 32 bits of addr. to bits 31–0 and compare
3	L	L	60	20	H	VBC_HM,E	042D 0000	Set Highest Match to “Empty”

Delete an Entry - Total Time=220ns

SYSTEM SUPERVISORY ROUTINES

These routines are included to aid the system in keeping track of the active addresses in the system, such as a shadow table stored in system memory. The Set Address Register routine needs only to be run once to initialize the Address register for a group of reads. Each read of the CAM will increment the Address register automatically, so the next read will access the next address in the CAM. The Page address needs to be set each time the Read Entries routine is run. The timing analysis assumed the worst-case scenario of 12 DA routines, 12 SA routines, 1 Management routine and 1 Read Entry routine per arbitration cycle, which must complete within one minimum length frame, which is 6.2 µs. The worst-case timing is 5.9 µs, which gives the arbiter 15 clock cycles to play with.

The Read Entry routine must be repeated for each address in each device. Because the associative memory locations of Next Free, Highest Matching, and All Matching are used to add and delete entries from the CAM, not all locations will contain valid data. The Status register contains the validity status of the CAM location that was just read, so Status register bit 29 and bit 28 must be checked. These bits will both be LOW for a Valid location.

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31-0] (HEX)	Description
1	L	L	20	20	H	SBR	0619 0000	Select Background Register Set
2	L	L	20	20	H	TCOW_AR	0A20 aaaa	Target Address Register on bits 31–16 Address value on bits 15–0
3	L	L	20	20	H	SFR	0618 0000	Select Foreground Register Set

Set Address Register - Total Time=120ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	L	L	20	20	H	SBR	0619 0000	Select Background Register Set
2	L	L	20	20	H	TCOW_DS	0A28 pppp	Target Device Select Register on bits 31–16 Page Address value on bits 15–0
3	H	H	60	20	H		dddd dddd	Data Read, Lower 32 bits
4	H	H	60	20	H		dddd dddd	Data Read, Upper 32 bits
5	L	H	40	20	H		dddd dddd	Command Read, Status Register
6	L	L	20	20	H	TCOW_DS	0A28 FFFF	Target Device Select Register on bits 31–16 Select all devices on bits 15–0
7	L	L	20	20	H	SFR	0618 0000	Select Foreground Register Set

Read Entries - Total Time=380ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
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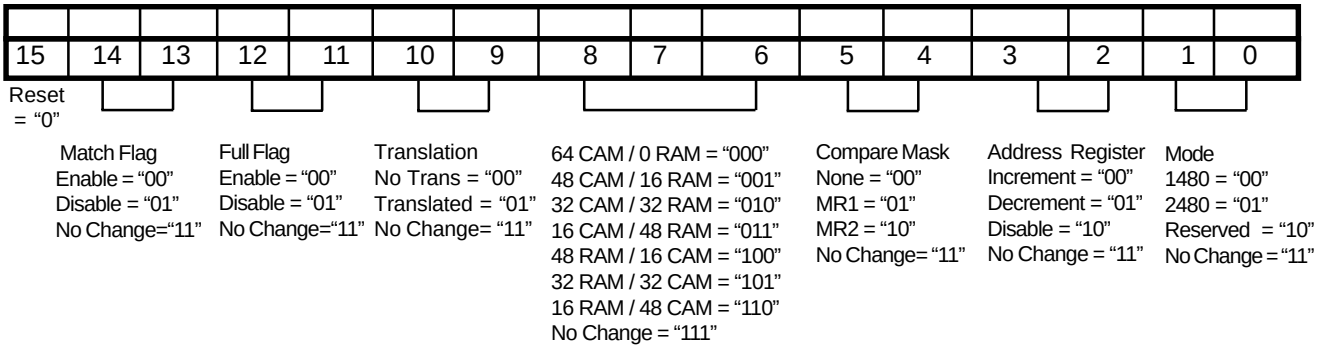
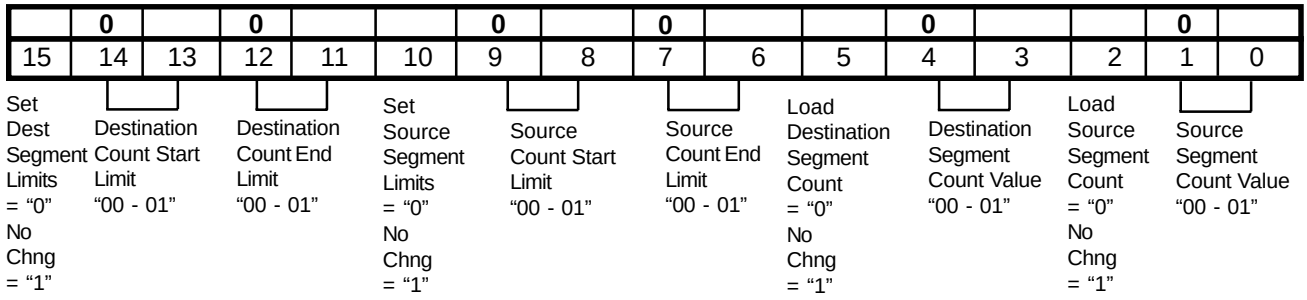
Blank Routine Worksheet



Control Register Bit Assignments



Segment Control Register Bit Assignments

NOTES

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