VPI/VCI Translation and Cell Tagging in ATM with the MU9C4320L ATMCAM™

INTRODUCTION

The MU9C4320L ATMCAM is a 4K x 32 content-addressable memory (CAM) with a 32-bit wide data interface. The device is designed for use in ATM switches and routers to provide very high throughput VPI/VCI translation. VPI/VCI fields from the ATM cell header are compared against a list of current connections stored in the ATMCAM array. As a result of the comparison, the ATMCAM generates an address that is used to access an external RAM where VPI/VCI mapping data and other information associated with the connection are stored.

ATM APPLICATIONS

VPI/VCI Translation

ATM global data exchange is based on a succession of point-to-point connections. Each of the connections is identified by a Virtual Path Identifier (VPI)/Virtual Channel Identifier (VCI) combination, which can be found in the header of all ATM cells carrying information for a specific connection.

At the User-Network Interface (UNI), the VPI is an 8-bit field and the VCI is a 16-bit field in the cell header, while at the Network-Network Interface (NNI) the VPI is a 12-bit field and the VCI a 16-bit field.

A VCI/VPI value strictly has local significance. Each segment of a total connection over several switches has unique VPI/VCI combinations for each segment of the connection, either from user to switch or from switch to switch. This implies that whenever an ATM cell travels through a switch, the VPI/VCI value has to be changed into the value used for the next part of the connection. This process is called VPI/VCI translation.

Various solutions can be implemented to perform such translations. Using the MU9C4320L ATMCAM is the most efficient solution and provides the following advantages:

- No limitation of the range of legal values for VPI/VCI, a guarantee for full interoperability
- Fully deterministic translation time, independent from the size of the list, and the length of VPI/VCI
- Automatic full VPI/VCI or VPI only translation without extra cycle
- Fast connection addition/deletion
- No limitation in terms of associated information to each connection.

Cell Tagging

In most switch implementations, the VPI/VCI translation is performed at the moment the ATM cells have been received by the switch port. In many designs, in addition to the VPI/VCI translation, the cells are tagged with information to route them through the switch. The cell tagging process can be handled by the ATMCAM during the VPI/VCI translation, without time penalty.

Policing

Besides VPI/VCI translation and cell tagging, a switch port may have to perform more functions which can be assisted by the ATMCAM. One of these functions is policing. With the help of the ATMCAM, the switch is able to check whether the VPI/VCI is known and a VPI/VCI translation and tagging operation can take place, or whether the cell should be discarded due to an unknown VPI/VCI.

The amount of cells that are allowed to come in during a certain time frame is based upon the bandwidth allocation for that specific connection. The average bandwidth and burstiness of the incoming cells for a connection have to conform to certain rules. If these rules are violated the switch could decide to drop the extra cells from that specific connection.

Alternatively those extra cells can still be forward by the switch. In such cases, their Cell Lose Priority bit (CLP) is updated. This field is part of each ATM cell header, and indicates if the cell is or is not within the negotiated bandwidth for the connection and its relative priority. If a burst of data traffic is happening and a specific switch is saturated, cells with a low priority will be dropped. Checking the value of the CLP field while processing the VPI/VCI

translation is easily done with the MU9C4320L, without requiring an extra cycle. It should be mentioned that this allows easy management of the incoming frame buffer in a "Find and Replace" mode.

SYSTEM BLOCK DIAGRAM

ATMCAM Controller

A wide variety of interfaces between ICs is found in the market today, not only varying in speed and type of information carried, but also varying in width. A possible ATM system is depicted in Figure 1. In this example system, a 16-bit wide UTOPIA (Level 2) interface (Cell Input and Output) is used.

The UTOPIA interface accepts cell data from a PHY device through the Cell Input interface. Transfer of cell data begins with the PHY device indicating it has data available for transfer by asserting the RxEmpty signal. Data is transferred over RxData15–0 in 16-bit quantities in each cycle following an assertion of RxEnb by the UTOPIA interface. Also transferred are RxSOC, the Start Of Cell indicator, and RxPrty, which provides odd parity over the 16-bit data bus.

Cell data is transferred from the UTOPIA interface to a downstream ATM Layer entity, such as the switch fabric or another UTOPIA interface, utilizing the Cell Output interface. The UTOPIA interface acts as a PHY device on the UTOPIA bus during transfer. Data is transferred over TxData15–0 in 16-bit quantities in each cycle following an assertion of TxEnb

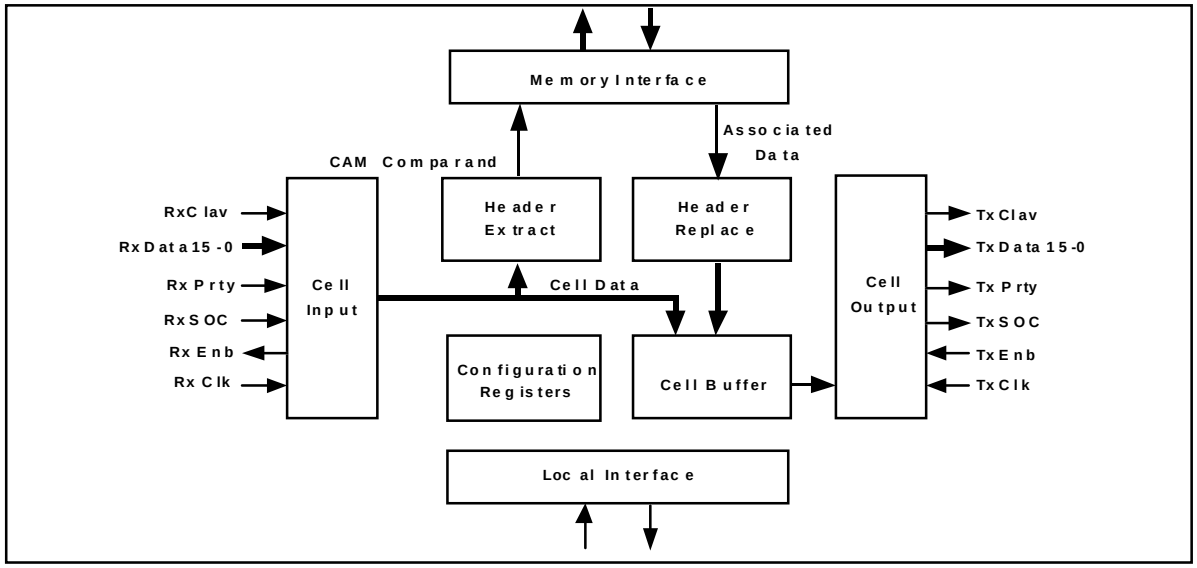

Figure 1: ATMCAM Controller, Block Diagram

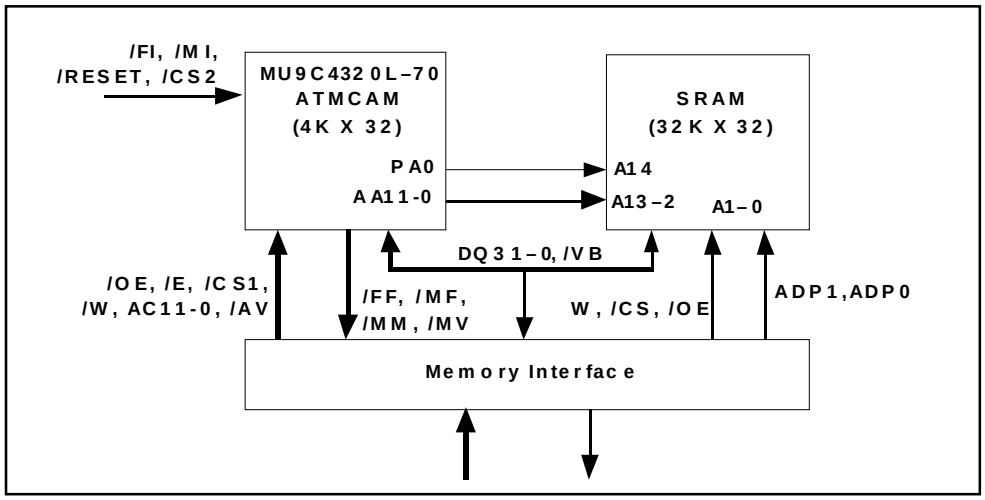

Figure 2: Memory Interface

by the controlling entity on the UTOPIA bus. Also transferred are TxSOC, the Start Of Cell indicator, and TxPrty, which provides odd parity over the 16-bit data bus.

Memory Interface

In Figure 2, the Memory interface is shown more precisely. The VPI/VCIs and VPIs are stored in the 70ns ATMCAM (MU9C4320L–70), associated data (new VPI/VCI or VPI and tagging information) is stored in a SRAM. 4K VPI/VCIs and 4K VPIs require 8K of SRAM containing the associated data. It is assumed that 128 bits of associated data per connection are required, so a 1Mb SRAM (8Kx128) is needed. Since 32-bit can be considered as a standard buswidth, in this example a 32K x 32 SRAM is used. This implies that the associated datafield has to be read out in four 32-bit parts.

The Page address of the ATMCAM or the VP Table is present on the PA bus. By choosing the Page addresses such that they only differ one bit (e.g. PA of the ATMCAM is 0000B and PA of the VP Table is 0001B) only one line of the PA bus has to be connected to the SRAM. In this example PA0 of the ATMCAM is used to address the SRAM and is therefore connected to A14 of the SRAM. When PA0 is "0" (ATMCAM), the first 16K of the SRAM are addressed and when PA0 is "1" (VP Table) the second part of 16K is addressed.

The AA bus presents the address of the matching location in the ATMCAM, or in case of a VPI match, the VP Table address. The AA bus is connected to the A13–A2 pins of the Address bus of the SRAM. By toggling the two least significant bits of the Address bus (A0 and A1) with external logic (or a burst counter internal to the SRAM), the associated data can be read out in four 32-bit parts.

An ATMCAM lookup requires 70ns (MU9C4320L–70). When using a standard 50MHz clock, it takes four 20ns clock cycles to perform a VPI/VCI lookup. To obtain maximum performance the lookup of associated data has to take place while the next ATMCAM lookup is performed. This implies each read operation of 32 bits of associated data has to be done within a 20ns clock cycle.

ATMCAM OPERATIONS

The flowcharts and code in this section are examples of the basic ATM operations in addition to the initialization of the ATMCAM:

- VPI/VCI lookup
- VPI lookup
- VPI/VCI addition
- VPI addition
- VPI/VCI removal
- VPI removal

```
!HARDWARE RESET
!MU9C4320 is in SW-mode

WR FR {MR000}                    /AV=HIGH      /W=LOW
0x00FFF100                       /AV=HIGH      /W=LOW
!MU9C4320 is programmed to HW-mode
!lowest priority CAM
!VP-table enabled
!VP PA is 1H
!PA is OH

WR DS {MR000}                    0x00000100    /AV=HIGH
!disable Device Select register CS

WR MR001                         0x0000000F    /AV=HIGH
!Mask register 1 for VPI/VCI

WR MR002                         0x000FFFFF    /AV=HIGH
!Mask register 2 for VPI
```

Figure 3: INIT.DAT, Initialization Code Listing

The format of the routines shown if the Code listings are as follows:

first column	: command on the AC bus
second column	: data on the DQ bus
third column	: the state of the AV pin

Initialization

The initialization routine shown in Figure 3 is called INIT.DAT. After a hardware reset the ATMCAM is in software mode. First the ATMCAM has to be programmed into hardware mode. The first two instructions take care of this. These two instructions also program the device as lowest-priority ATMCAM, enable the VP Table, set the VP Page address to 1H, and set the ATMCAM Page address to 0H.

Lookup

The VPI/VCI lookup is done in routine LOOKUP.DAT, shown in Figure 5 (flowchart in Figure 4). At the end of this routine the flags /MV and /MF indicate whether a match occurred or not and if so what kind of match it is. For a VPI/VCI matching, the matching address will be present on the AA bus, the PA bus will present the PA of the ATMCAM (0H). If there was a match in the VP Table and not in the ATMCAM the matching VP Table address will be present on the AA bus, the PA bus will present the PA of the VP

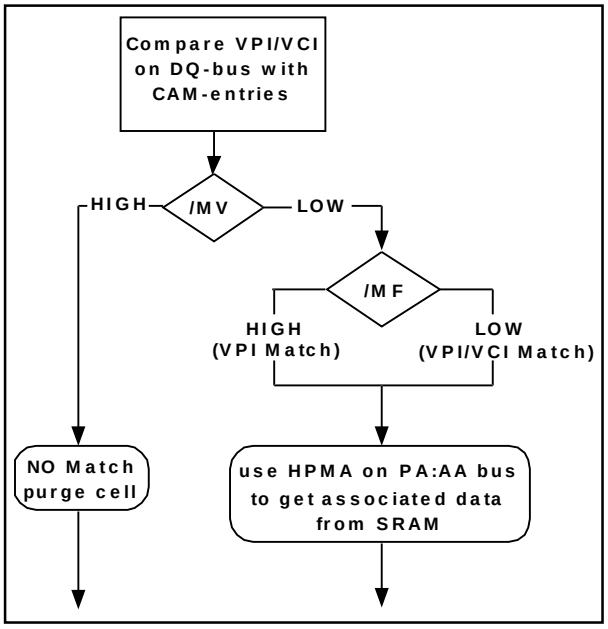

Figure 4: Lookup Flowchart

```
CMP DQ {MR001}      VPI/VCI                 /AV=HIGH
!compare VPI/VCI
```

Figure 5: Lookup.Dat, VPI/VCI Lookup Code Listing

```
CMP DQ{MR002}       VPI                     /AV=HIGH
!compare only VPI
```

Figure 6: VPI Lookup Code Listing

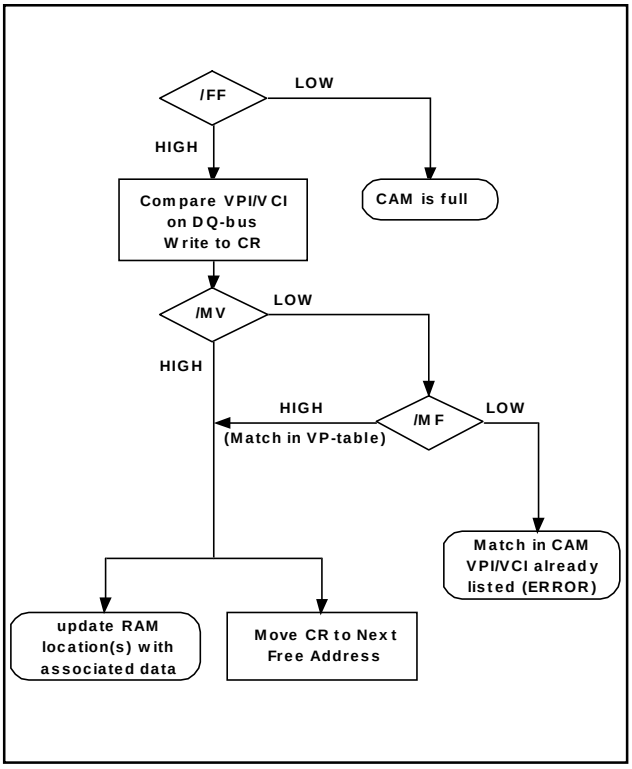

Figure 7 : Add a VPI/VCI-connection

```
CMPW  DQ {MR001}VPI/VCI       /AV=HIGH
!compare VPI/VCI and write it to CR

MOV [NFA], CR {MR001}         /AV=HIGH
!move the content of CR to the Next Free Address
```

Figure 8: ADD.DAT, Add a VPI/VCI-connection Code Listing

Table (1H). The SRAM can be addressed by a combination of the PA bus, AA bus, and some external logic to read out associated data. If a lookup on only the VPI is required, use MR002 instead of MR001 and write the VPI on the DQ bus (see Figure 6).

Adding a Connection

To add a VPI/VCI to the list in the ATMCAM, the routine ADD.DAT is used. This routine is shown in Figure 8 (flowchart in Figure 7). It first compares the VPI/VCI to be added. In this example switching on VPI/VCI is allowed also if the VPI of this connection is already set in the VP Table (so it is possible to switch separate VCIs of a VPI connection). This means a VPI/VCI connection can be added when it is not found in the ATMCAM. To add the VPI/VCI it is moved from the Comparand register to the Next Free address. This NFA becomes available at the PA:AA bus, so the SRAM can be addressed to write the associated data into it.

To add a VPI the routine used is ADD_VPI.DAT, which is shown in Figure 9. First a lookup on the VPI is performed. Since in this example it is possible to switch certain VCIs separate from a VPI connection, the VPI is added if it is not already set. In other systems where it is not allowed to switch on separate VCIs, the decision to add the VPI and delete the VPI/VCIs conflicting with this VPI can be taken by external logic, as shown in Figure 10. Addition of the VPI is done by writing the VPI to the Address register, after which the corresponding VP Table address is set.

```
WR AR {MR000}          VPI              /AV=HIGH
!write VPI to AR

SET VP@[AR]                             /AV=HIGH
!set VP Table bit at AR-location
```

Figure 9: Add_VPI.DAT. Add a VPI connection Code Listing

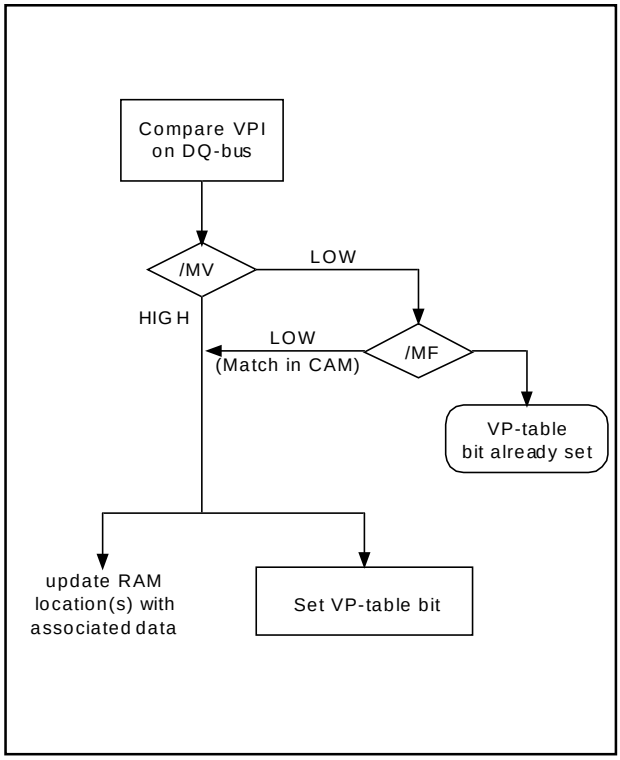

Figure 10: Alternative Method to Add a VPI connection

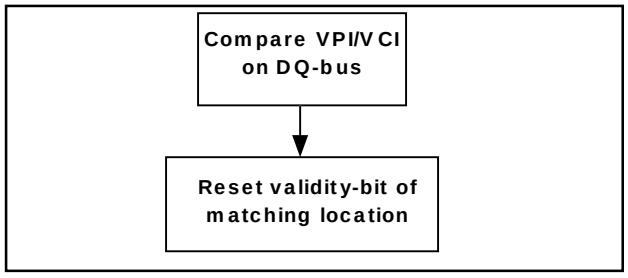

Figure 11: Delete a VPI/VCI connection

```
CMP  DQ {MR001}        VPI/VCI  /AV=HIGH
!compare VPI/VCI

RST V@[HPM]                             /AV=HIGH
!reset validity-bit at Highest Priority Matching location
```

Figure 12: DELETE.DAT, Delete a VPI/VCI connection Code Listing

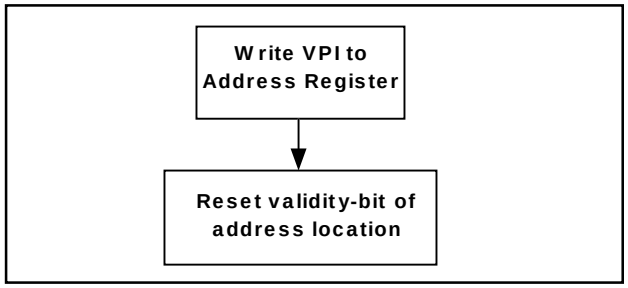

Figure13: Delete a VPI connection

```
WR AR{MR000}           VPI              /AV=HIGH
!write VPI to AR

RST V@[AR]                              /AV=HIGH
!reset VP table bit at AR-location
```

Figure 14: Delete_VPI.DAT, Delete a VPI connection Code listing

Delete a Connection

To delete a VPI/VCI from the ATMCAM list, routine DELETE.DAT is used. It is shown in Figure 12 (flowchart in Figure 11). First the VPI/VCI is looked up in the ATMCAM to obtain the address of the connection to be deleted, after which the VPI/VCI can be deleted by resetting the Validity Bit of the matching location.

To delete a VPI from the VP Table, routine DELETE_VPI.DAT is used. It is shown in Figure 14 (flowchart in Figure 13). The VPI is written to the Address register, after which the corresponding bit of this VPI value in the VP Table is reset.

Neither deletions require any action with the associated data in the SRAM, because these locations will not be addressed by the ATMCAM anymore.

TIMING IMPLICATIONS

All basic operations of the ATMCAM require short cycles of /E (35ns LOW time and 15ns HIGH time). The compare operation however requires a long cycle of /E (55ns LOW time and 15ns HIGH time). So when using a 50 MHz clock all operations take 60ns except for the compare, which takes 80ns. A fast SRAM can perform read-or-write-operations within one clock cycle. So to translate a VPI/VCI, the first four clock cycles for lookup are required, after which the associated data is being read in four times one cycle. So a translation would take only 160ns. The ATMCAM is a pipelined device. The data on the output (PA:AA bus) will remain stable until the next data is looked up and the result is available after the rising edge of /E. This means that while addressing the SRAM the next lookup in the ATMCAM can be started. An effective translation time of 80ns is achieved by doing so. An overview of the time required for the basic ATM operations is given in Figure 15.

VERTICAL CASCADING THE ATMCAM

An important feature of the ATMCAM is its cascadability. The system can be designed to any practical depth by vertically cascading ATMCAMs. The scheme uses a daisy chain to provide system-level prioritization as well as Match, Multiple match, and Full flags. There are three daisy chains: Match, Multiple match, and Full, plus a Match Valid line indicates both the CAM and VP Table matches.

When a control state is broadcast that accesses the highest-priority matching location or Status register, the daisy chain ensures that the only device that responds is the one with the highest-priority match in the system. All other devices will have their DQ31–0 lines and PA3–0: AA11–0 outputs held in high impedance. Therefore, the Match Flag daisy chain controls access to the system resources for control states that are conditional on all the results of the previous Compare cycle.

During a Comparison cycle, the Match and Multiple Match flags will not change until /E goes High during that cycle. At this time, the daisy chain starts to resolve system-level prioritization. Once sufficient time has elapsed for the daisy chain to be resolved, the PA3–0:AA11–0 lines can be enabled with /OE, and Status register Read cycles will access only the highest-priority matching device. Note that the daisy chain resolves system-level prioritization combinatorially once initiated by /E going HIGH. Other cycles that do not affect the daisy chain or match results can take place in the ATMCAM while the daisy chain is resolving, for example, WR CR, allowing some degree of pipelining. During a Write cycle, the Full flag will not change until /E goes HIGH during that cycle.

Operation	T [CLK-cycles]	T [ns]	see Figure
lookup a VPI/VCI or VPI	4	80	Figure 18
adding a VPI/VCI	4 +3 = 7	140	Figure 19
adding a VPI	3 + 3 = 6	120	Figure 20
removing a VPI/VCI	4 + 3 = 7	140	Figure 21
removing a VPI	3 + 3 = 6	120	Figure 22

Figure 15: Time required for basic operations

There is a small propagation delay per device in the daisy chain. Alternatively, vertical cascading can be done with external logic that provides prioritization and select lines back into each device. The ATMCAM architecture supports external prioritization for cases where the daisy chain overhead proves unacceptable. Figure 16 shows a system in which a number of ATMCAMs are vertically cascaded.

Full Cascading

The Full flag is set LOW in a particular ATMCAM if the /FI line is LOW and that device is full. During a Write cycle, the Full flag will not change until /E goes HIGH during that cycle. When the /FI line is HIGH, one or more locations are free in the higher-priority devices; therefore, when the /FI line is HIGH, whether or not that particular device is full, its /FF output will remain HIGH. This method allows the Full Flag daisy chain to recognize non-contiguous empty locations throughout the entire ATMCAM system.

The daisy chain gives System Full indication. When the device at the end of the chain has its /FF output LOW the entire CAM system is full. The first device in the daisy chain has its /FI line tied LOW to ensure data can be written into the system.

The daisy chain also controls Write at Next Free Address cycles as well as Read Next Free Address cycles so that they work globally across the system, and not just locally in a specific device. Only the device in which the /FI line is LOW, and which is not full, will respond to the Write cycle. Therefore, deletions and insertions can be made in the memory, without the need to keep track of empty locations.

Match Cascading

The Match flag, /MF will be LOW in a particular device within a vertically cascaded system when its /MI input is LOW, or when there is a match in that device. During a Comparison cycle, the Match flag will not change until /E

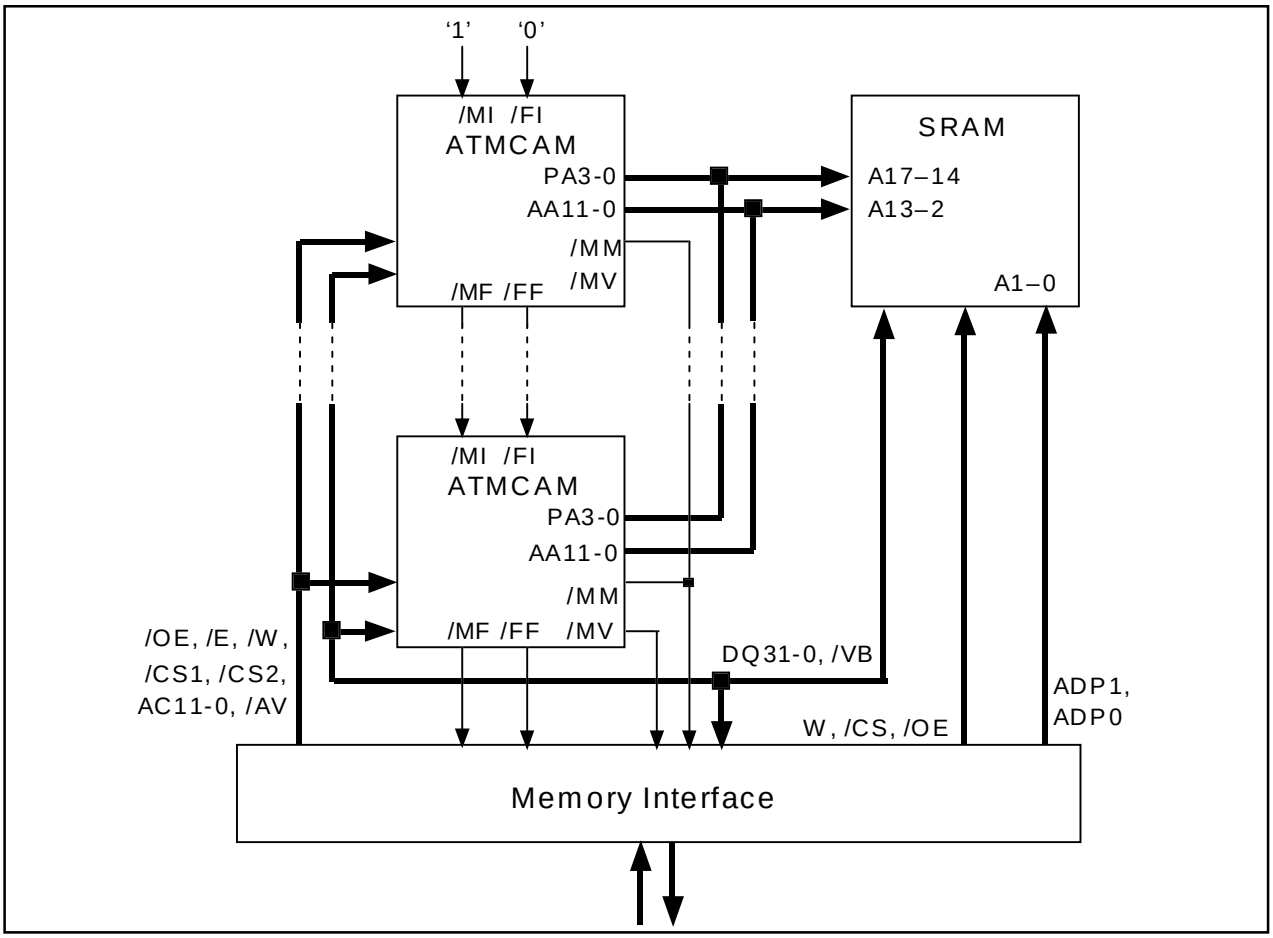

Figure 16 : Memory Interface using Vertically Cascaded Devices, Block Diagram

goes HIGH during that cycle. When the /MI line is LOW, one or more locations in higher-priority devices have a match; when the /MI line is LOW, the /MF output will be forced LOW. This method allows the Match Flag daisy chain to respond to and prioritize matches throughout the entire ATMCAM system.

The daisy chaining gives a System Match indication. When the device at the end of the daisy chain has its /MF output LOW there is a match within the CAM system. The first device in the daisy chain has its /MI input tied HIGH.

The daisy chain also controls access to the device by controlling the outputs during a Read Highest-Priority Match data, or Read Status register, onto the DQ31–0 lines. The device must be selected with either /CS1 or /CS2 or the Data Select register. After a Comparison or Read/Write at Highest-Priority Match Address cycle, only the device whose /MI line is HIGH, and which has a valid match, will drive data onto DQ31–0 or onto PA3–0:AA11–0; any device that has its /MI line set LOW will have its outputs in their high impedance state, even if it has a valid match. Therefore, Reads from and Writes to the highest-priority matching address operate over the entire system; only the device in which the /MI line is HIGH and which has a match will respond to the cycle. This scheme automatically prioritizes a system of vertically cascaded devices, the highest up in the chain has the highest priority. Note, however, that cycles which do not access highest-priority match data or the Status register will operate without regard to the state of the Match daisy chain.

Multiple Match Flag Daisy Chain

The Multiple Match flag, /MM, is an open-drain output and will be pulled LOW by a particular device when its /MI input is HIGH and there is more than one match within the device, or when the /MI input is LOW and there is one match within the device. During a Comparison cycle, the Multiple Match flag will not change until /E goes HIGH during that cycle. This wireORed output provides system level indication of the multiple match condition within a vertically cascaded system of ATMCAMs.

Match Flag Timing Overhead

There is a propagation delay for the match results to ripple down through the daisy chain. All the ATMCAMs within the system execute a Comparison cycle in parallel, so the local results are available at the end of a Comparison cycle. The local match flags do not change during a Comparison cycle until /E goes HIGH. The logical combination of the results then propagates down the daisy chain with a delay through each stage. The compare time in each device operating in parallel is added to the ripple delay through the daisy chain. Before reading the results of a comparison from the System Match flag, the daisy chain must be given time to settle to a valid state. If there are N devices vertically cascaded in a system, and the time to get a valid output on /MF for one device is t(MF), and the propagation delay for the flag to ripple through one device from /MI valid to /MF valid is t(PD), then the time t(DC) for the daisy chain to develop a valid output condition is:

$$t(DC) = t(MF) + (N-1) \bullet t(PD)$$

This period of time must elapse before the flagged results of the comparison are available, and before /OE is driven LOW or a Status register Read cycle is performed.

There is a similar but shorter delay for the Full Flag daisy chain, but this just limits the rate at which back-to-back Write at Next Free Address cycles can be performed.

External Prioritization

For systems where the propagation delay associated with the Match Flag daisy chain is unacceptable, the ATMCAM supports external prioritization. For external prioritization, the /MI input is connected through the AND gate to /MF outputs of all the higher-priority devices. This configuration shortens the path from any /MF output to any lower-priority /MI input, and allows the IE, /CS, and /OE inputs to operate in their normal manner.

In Figure 16 the Memory interface of a vertically cascaded system is depicted. It is important to note that only one ATMCAM can contain the VP Table. In Figure 16 the last device contains the VP Table, so the Match Valid line of this device is the only /MV that needs to be connected to external logic. Only in this device can a match in ATMCAM and VP Table occur. During initialization the Page address of each ATMCAM and the VP Table are set to an unique value. If the devices in a vertically cascaded system are to be selected solely through the Device Select register, then the Page addresses must be set to unique values in each device. However, to set the Page address in each Configuration register in turn would require that each device already have a unique Page Address value. To overcome this dilemma, there are two special control states that allow the Page Address registers to be set individually in this circumstance. Once the general operating conditions are

established by broadcasting a configuration value to all the ATMCAMs in the system, the Page Address values must be set to a unique value in each device. This is done through a sequence of WR PA control states, each executed with a unique value on the DQ3–0 lines. This control state writes the DS3–0 value into the Page Address field of the Configuration register of the highest-priority empty device, and then sets the Full flag of that device to indicate Full (LOW). The next WR PA will therefore be directed to the next lower-priority device within the system. The sequence continues until all Page Address values have been written. The RST FF control state is then broadcast to all devices to set the Full flags back to empty, and the system is then ready for normal operation. Now each device has a unique Page address and the VP Table of one device can be set. To do so select this device and write the new settings to its Configuration register. Now only the mask registers need to be programmed and the initialization of the vertically cascaded system is finished. See Figure 17 for the Code Listing of the initialization routine (CASC_INIT.DAT) of a vertically cascaded system.

CONCLUSION

The MU9C4320L ATMCAM is very well suited for use in a wide range of ATM systems. Since basic operations are being performed in limited time it is possible to use the ATMCAM in today's state of the art ATM switches with the possibility to multiplex ATM streams. Also in backbone applications where long lists (more than 8K entries) are used, vertically cascading the ATMCAM to any practical length can be used in long list systems, such as backbones.

```
!HARDWARE RESET
!MU9C4320 is in SW–mode
                                                    /AV=HIGH        /W=LOW
WR FR {MR000}
0x03000000                                          /AV=HIGH        /W=LOW

!MU9C4320 is programmed to HW-mode

! ------------------------------------------------------------------------

WR PA                           0xXXXXXX0           /AV=HIGH

!set PA of Highest Priority Empty Device to 0H

!the Full Flag of this device becomes active so the next device in the chain
 !becomes the HPEDevice

WR PA                           0xXXXXXX1           /AV=HIGH

!set PA of HPED to 1H

! ------------------------------------------------------------------------

! continue this until all devices are set with an unique Page Address.


RST FF
!reset all Full flags

WR DS {MR000}                   0x00000001          /AV=HIGH

!select the device with PA3–0 = DS3–0 (=1H)

!WR FR {MR000}                  0x01FFF201          /AV=HIGH

!in the selected device the VP Table is enabled and its PA is set to 2H

WR DS {MR000}                   0x00000100          /AV=HIGH
!disable Device Select Register

WR MR001                        0x0000000F          /AV=HIGH

!Mask Register 1 for VPI/VCI


WR MR002                        0x000FFFFF          /AV=HIGH

!Mask Register 2 for VPI
```

Figure 17: CASC_INIT.DAT, Code Listing

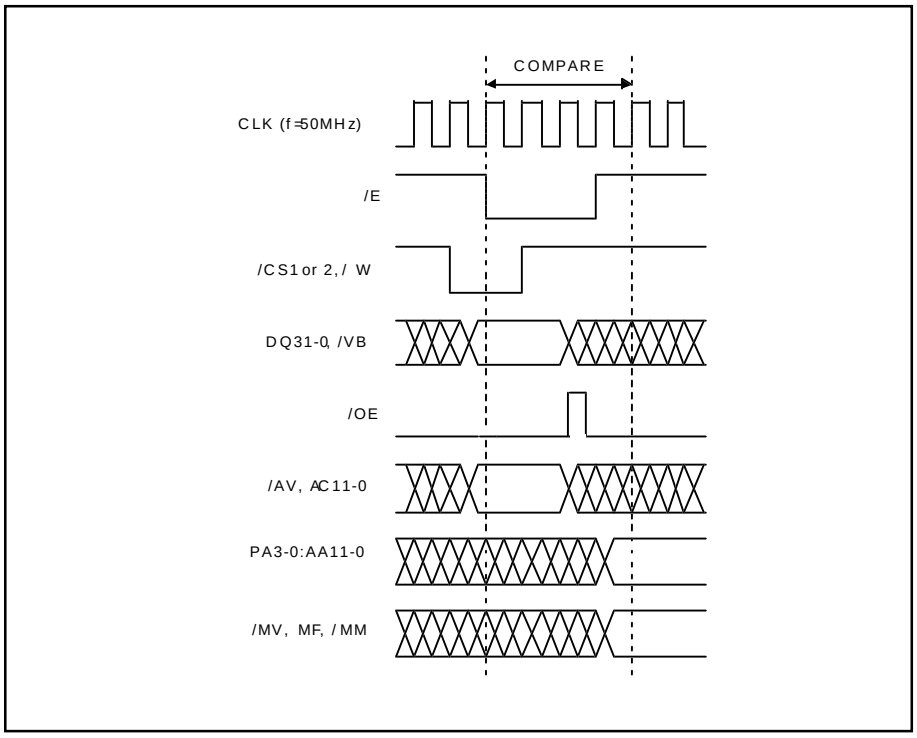

Figure 18: VPI/VCI Lookup, Timing Diagram

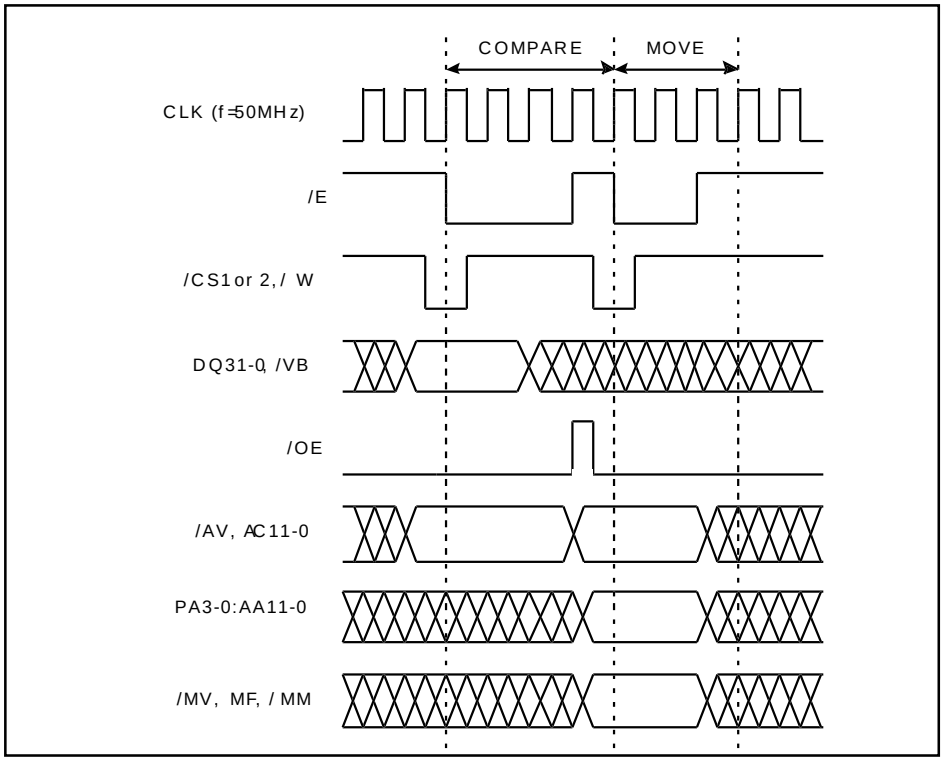

Figure 19: Add a VPI/VCI Connection, Timing Diagram

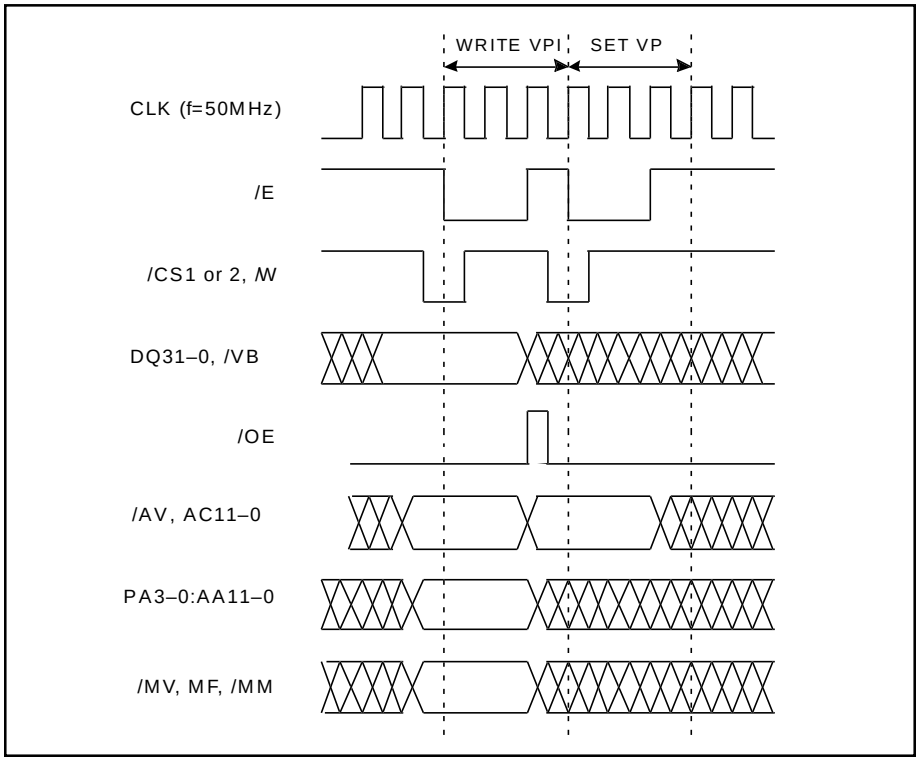

Figure 20: Add a VPI Connection, Timing Diagram

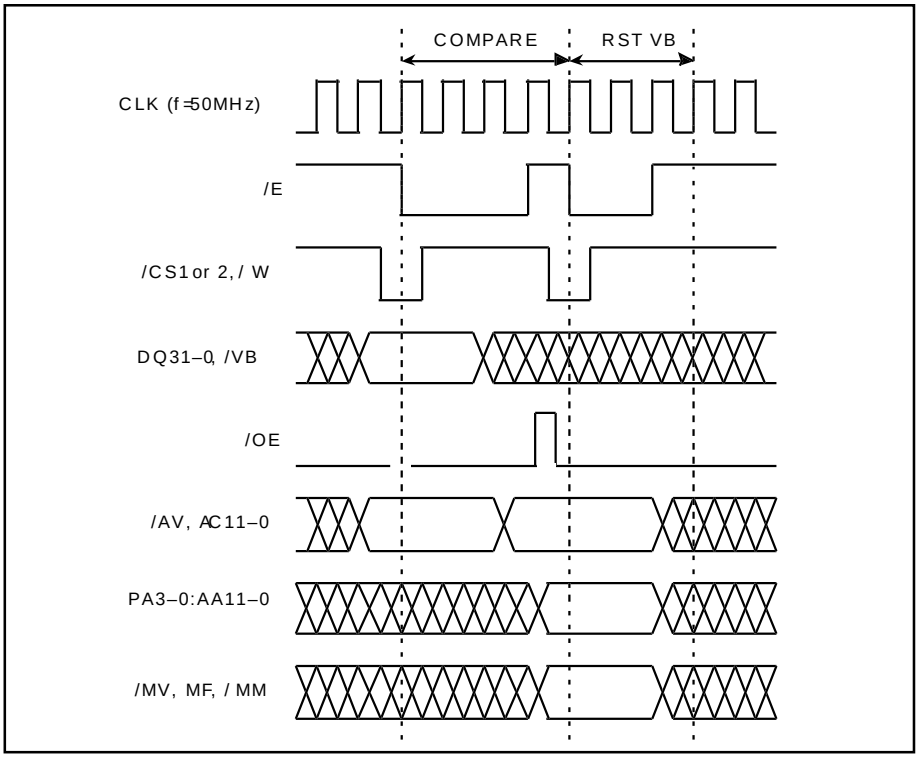

Figure 21: Delete a VPI/VCI Connection, Timing Diagram

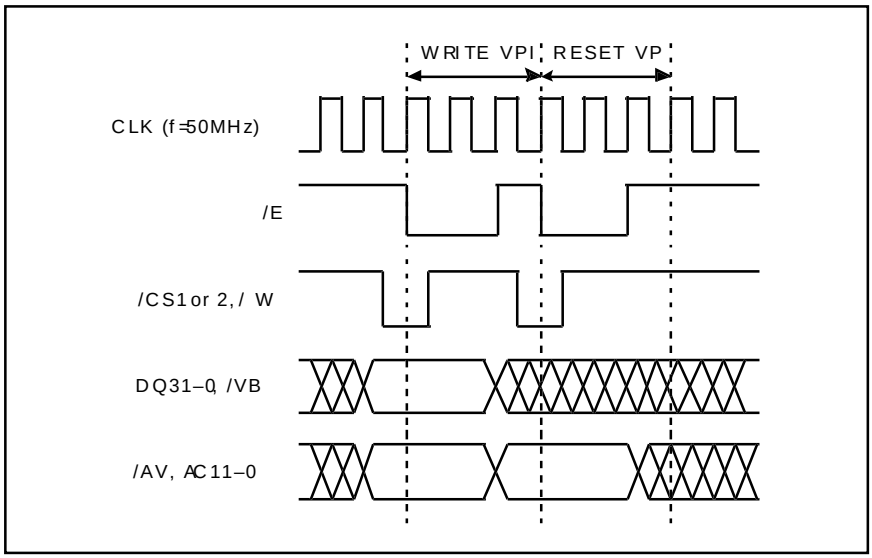

Figure 22: Delete a VPI Connection, Timing Diagram

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