Using The MU9C1485A/L WidePort LANCAM® For Address Filtering And Translation

INTRODUCTION

The MU9C1485A/L WidePort LANCAM is a 1024 x 64-bit content-addressable memory (CAM). It features a 32-bit bus, providing twice the I/O bandwidth over the MU9C1480A/L. This wider bus reduces the number of cycles required to write addresses to the Comparand register and read match results from the Status register, increasing the performance of address filtering and translation. Additionally, dedicated match and multiple match flag pins enhance hardware control of the device.

The MU9C1485A/L may be used to perform address filtering or translation operations in computer networks. Each 64-bit entry in the device can be programmed with either a 32-bit ATM or IP address or a 48-bit Ethernet, Token Ring, or FDDI address. Additional bits left over in each entry may be used for special functions such as aging or tagging.

All of the network address entries in the CAM constitute a database. This database is accessed by loading the device's Comparand register with the 32-bit or 48-bit address from a newly arrived communication packet. An automatic comparison is initiated after the loading of the Comparand register, giving three useful pieces of information:

1. Match and Multiple Match flags: the Match flag indicates the address was found in the database, and the Multiple Match flag indicates the address was found multiple times in the database. These flags are available on pins as well as in the device's Status register.
2. Match address: the Match address, stored in the Status register, gives the specific location of the particular entry that matches the Comparand register contents. This is useful for accessing any associated data fields kept in an external RAM table.
3. Associated data: part or all of the matching location in memory may be read back, allowing access to internal associated data, another name for data stored with a particular matching location.

There are a total of 1024 entries in the MU9C1485A/L. Each entry is 64 bits in width. Databases with more than 1024 entries may be constructed by connecting multiple devices to common data and control buses. In such a database, the Full and Match flags (/FF and /MF) are connected in a daisy-chained manner. An example of a 4096-entry database is given in Figure 1.

The Full flag daisy chain provides prioritization across devices when a new entry is to be written to the Next-free location in the database. Likewise, the Match flag daisy chain provides prioritization of multiple matches when the matches reside in different devices. Multiple matches within a single device are prioritized by the device's Priority encoder. The Full and Match Flag outputs from the last device may be used as System match and Full flags.

The rich MU9C1485A/L instruction set and dual mask registers can be used to construct a wide variety of custom routines. Maintenance of the CAM database is made simple

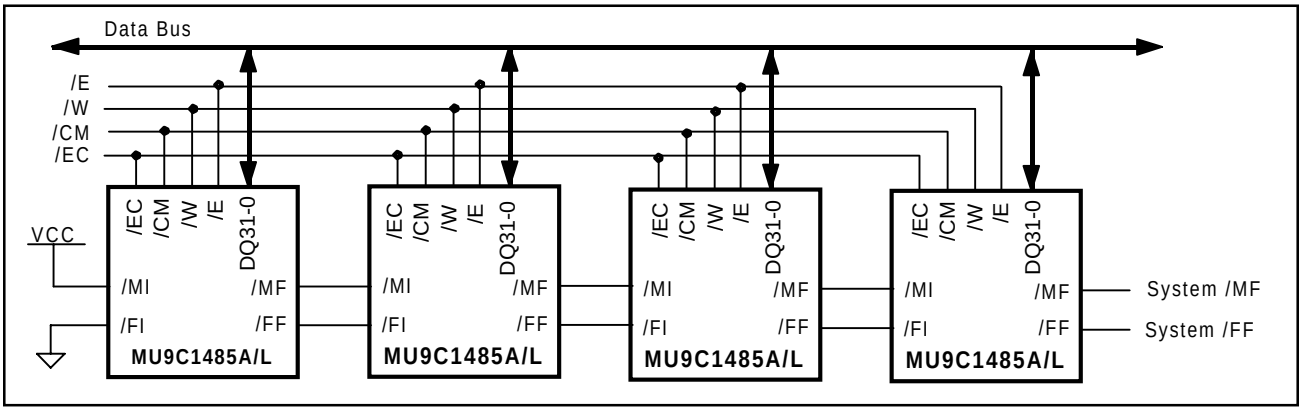


Figure 1: 4096-entry Daisy Chained MU9C1485A/L Database

Note: This document version has not completed MUSIC's internal approval process, therefore it should be rechecked with a released version or with factory personnel.

with instructions such as MOV NF,CR,V which allows a new entry to be written to the next free location in the CAM. Multiple entries associated with a matching identifier may be deleted by using the instruction VBC ALM,E. This sets all locations that currently match the Comparand register to an "Empty" validity state. Multiple entries with a common parameter, such as port ID or time stamp, may be deleted simultaneously using this instruction.

INTERFACING

Typically, a state machine PLD or ASIC is used to drive the MU9C1485A/L, allowing maximum efficiency for the address filtering or translation function. The state machine is used to drive different length /E cycles to the device. Figure 2 shows the timing for a state machine that drives the MU9C1485A/L with short, medium, and long cycles based on one, two, or three cycles of its input clock. The actual clock frequency used will depend upon various factors such as the CAM's tELEH timing parameters, state machine operating frequency constraints, and any considerations for maintaining synchronous operation with other clocks in the system.

The first and second cycles in the example are a Command write and read, respectively. The control signals are setup one cycle prior to the falling edge of /E and are maintained through the duration of the /E low period. This ample setup and hold time for the control signals. The third cycle is a Data write with /EC taken low. This type of cycle is typically used for the last write to the Comparand register that initiates an automatic compare. The daisy chain is locked in the following CAM cycle, allowing a read of status or associated data from the highest-priority matching device. A range of system clock frequencies may be used to drive the MU9C1485A/L LANCAM, depending on the device speed grade chosen. Short, medium, or long cycles are controlled by the LOW time of /E. Different operations will require different times to complete.

Table 1 shows an example of timing templates for various length cycles of /E low, corresponding to the tELEH data sheet parameter. These example cycle periods are given for clock frequencies from 20MHz to 66 MHz. Short, medium, and long CAM cycles are constructed from one to seven clock cycle periods.

The state machine controlling the /E input might have a "clock to output LOW" time that is longer than its "clock to output HIGH" time. Under this condition, care will have to be exercised if the short, medium, or long period works out to the exact same number as the tELEH AC parameter of the MU9C1485A/L. This would result in a tELEH time that is in violation of the specification. Using a slightly lower clock frequency, adding an extra clock cycle, or adding a pulldown resistor to the controlling device's output can remedy this situation.

The period /E remains HIGH between CAM cycles is dependent on the type of CAM operation performed in the previous CAM cycle. If a non-compare cycle was just executed, the minimum /E HIGH time used is simply the tEHEL parameter in the data sheet. However, if a comparison was just executed, the /E HIGH time must be lengthened to allow the match flags in the system to settle. This is required to ensure correct access to the CAM with the highest-priority match.

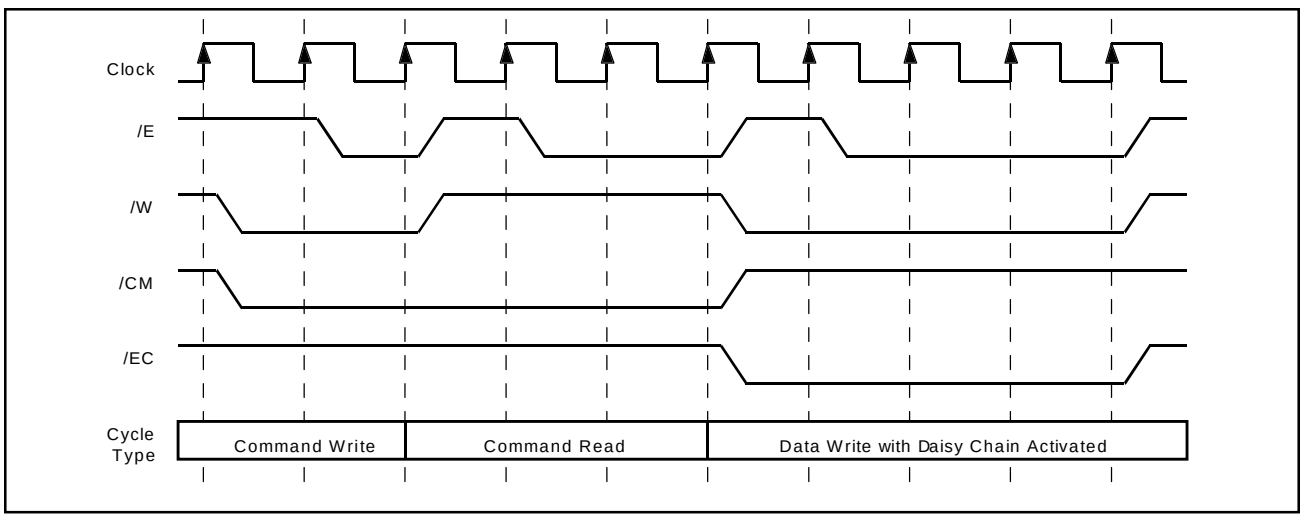


Figure 2: State Machine Driven Short, Medium, and Long CAM Cycles

Clock Freq. (MHz)	Clock Period (ns)	Short tELEH Clock Cycles	Medium tELEH Clock Cycles	Long tELEH Clock Cycles	Short tELEH *Period* (ns)	Medium tELEH *Period* (ns)	Long tELEH *Period* (ns)	MU9C1485A/L Speed Grade
20.0	50.0	1	2	2	50.0	100.0	100.0	-12
25.0	40.0	1	2	3	40.0	80.0	120.0	-12
33.3	30.0	1	2	3	30.0	60.0	90.0	-90
33.3	30.0	2	3	4	60.0	90.0	120.0	-12
40.0	25.0	1	2	3	25.0	50.0	75.0	-90
40.0	25.0	2	3	4	50.0	75.0	100.0	-12
50.0	20.0	2	3	4	40.0	60.0	80.0	-90
66.7	15.0	2	4	5	30.0	60.0	75.0	-90
66.7	15.0	3	5	7	45.0	75.0	105.0	-12

Table 1: MU9C1485A/L /E LOW Cycle Time Examples

The tEHMFV timing parameter describes the time it takes for the Match flag to go valid once /E goes HIGH at the end of a comparison cycle. Also, in daisy-chained systems, the tMIVMFV parameter determines the time it takes for the Match flag to ripple through a single device. The daisy chain needs to settle before the next cycle is started. As such, the /E HIGH time should be greater than tEHMFV + (n-1)•tMIVMFV, where n is the number of CAMs in the daisy chain.

The MU9C1485A/L may also be directly connected to a 32-bit microprocessor bus, however lower performance will typically result. If this approach is used, the control signals (/E, /W, /CM, and /EC) can be decoded as unique addresses in the memory space. The MU9C1485A/L's DQ bus would be connected to the main data bus. If the data bus is heavily loaded, buffers may need to be inserted to guarantee the timing.

The DQ bus should be terminated with pullup resistors, particularly in the case of a daisy chain system. This ensures that if no CAM responds to a read of the Status register, the data bus will be in a determinant state. Pullup terminations are also important for reducing MU9C1485A/L power consumption when the DQ bus is left floating for long periods of time (e.g. microseconds). Typical values for the pullup resistors are 2.2 kohm to 10 kohm. The actual value selected will depend on capacitive loading and speed of operation.

The first device in a daisy chain should have its /MI pin tied HIGH, and its /FI pin tied LOW. This indicates to the first device that there are no higher-priority devices installed before it in the daisy chain. The Page Address register is used to give each device in a daisy chain a unique identity. A particular device is selected for individual access by writing the Device Select register with a value that matches the target device's Page Address register. Additionally, a Device Select value of FFFFH will select all devices for write operations, enabling broadcast operation.

If there is only one device being used in the system, the Device Select and Page Address registers should be set to the same value, and the /EC signal should be tied HIGH. This approach will disable the device prioritization feature present in daisy-chained devices and allow complete read and write access to the single device. Note that the /MF flag will be forced HIGH when /EC is tied HIGH. The /MA and /MM pins will still reflect the match status of the device, however.

CYCLE TIME COMPARISON

The MU9C1485A/L provides improved performance in network address filtering or translation over the MU9C1480A/L. Due to the MU9C1485A/L's 32-bit I/O bus, the number of cycles required to load the Comparand register with data is reduced, and instructions that require an absolute address or value take one cycle instead of two. Tables 1, 2, and 3 show the improved performance of the MU9C1485A/L over the MU9C1480A/L for time-critical applications. In each example, the timings assume -90 devices are used in Enhanced mode. Actual implementations will be governed by the clock cycle time available in the application. The abbreviations are DW=Data Write, DR=Data Read, CW=Command Write, CR=Command Read, DA=Destination Address, SA=Source Address, HMA=Highest-priority Match Address, NFA=Next Free Address, and VPI/VCI=Virtual Path Identifier/Virtual Channel Identifier.

Table 2 gives an example of translating an incoming 32-bit VPI/VCI address into an outgoing 32-bit VPI/VCI address, as might be done in an ATM switch. Masking can be used to reduce the address width to 24 bits or 28 bits as required. If an external RAM table needs to be addressed, a read of the Status register can be added to fetch the pointer. The same 32-bit CAM/RAM split can be used in disk cache

MU9C1480A/L (16-bit I/O)	Time	MU9C1485A/L (32-bit I/O)	Time
DW of VPI/VCI	40 ns	DW of VPI/VCI and Compare	90 ns
DW of VPI/VCI and Compare	90 ns	DR from HMA	90 ns
DR from HMA	90 ns		
DR from HMA	90 ns		
TOTAL	**310 ns**	**TOTAL**	**180 ns**

Table 2: A Typical 32-bit ATM VCI/VPI or Disk Cache Translation Application

MU9C1480A/L (16-bit I/O)	Time	MU9C1485A/L (32-bit I/O)	Time
DW of DA	40ns	DW of DA	40ns
DW of DA	40ns	DW of DA and Compare	90ns
DW of DA and Compare	90ns	DR from HMA	90ns
DR from HMA	90ns	DW of SA	40ns
DW of SA	40ns	DW of SA and Compare	90ns
DW of SA	40ns	CW of a Move to NFA	90ns
DW of SA and Compare	90ns		
CW of a Move to NFA	90ns		
TOTAL	**520ns**		**440ns**

Table 3: A Typical 48-bit Network Address Filtering Application

MU9C1480A/L (16-bit I/O)	Time	MU9C1485A/L (32-bit I/O)	Time
DW of DA	40ns	DW of DA	40ns
DW of DA	40ns	DW of DA and Compare	90ns
DW of DA	40ns	CR of Status Register	65ns
DW of DA and Compare	90ns		
CR of Status Register	65ns		
TOTAL	**275ns**	**Total**	**195ns**

Table 4: A Typical 64-bit E.164 Filtering Application

controllers, to translate between a cluster tag and the cluster location in cache memory. Again, masking can be used to reduce the tag width, or to allow for "don't cares," so that a value within a range of values can be found, such as a specific sector within a cluster stored in the cache. After the input data is loaded into the Comparand register, a Compare cycle occurs, and if there is a match, the translated output data is read from the associated data field at the Highest-Priority Match address.

Table 3 is an example of filtering a 48-bit network address (Ethernet, Token Ring, or FDDI) as might be done in a bridge, router, or switch. After the Destination address is loaded into the Comparand register, a Compare cycle occurs, and if there is a match, the 16-bit Associated Data field containing the output port number is read from the memory. Then the Source address is loaded into the Comparand register, a Compare cycle occurs, and if there is no match, the Source address is learned by moving it to the Next Free address in the device.

Table 4 shows the case of a 64-bit network address filtering operation, such as recognition of an E.164 address. In the case of a match, the Match address is read out of the Status register and used as a pointer to external RAM, where the routing information is stored.

EXTERNAL PRIORITY ENCODER

For additional performance in systems with multiple MU9C1485A/Ls, an external Match flag priority encoder may be used instead of the daisy-chained approach. The advantage of an external priority encoder is the serialized daisy chain propagation delay is avoided. Without the daisy chain propagation delay, the match status of the system is resolved more quickly, allowing the next cycle to begin sooner.

In daisy-chained systems, the /EC control input is brought LOW when a compare is initiated. The cycle following any cycle with /EC asserted is subject to the daisy chain's locking

effect. During this time, only the CAM with the highest-priority match will respond to command and data reads and writes. If no CAM has a match, then no device will respond.

The external priority encoder may be implemented in a PLD as shown in Figure 3. The internal match flags from all MU9C1485A/Ls, /MA3–0, are input to the PLD along with the /E signal, which determines the fundamental timing of CAM cycles. The /ELOCK control bit is used to determine whether the /E signal is broadcast to all CAMs or instead only enabled to the CAM with the highest-priority match. Additionally, the /SYSMF output provides a system match flag by logically ORing all of the /MA signals.

The external PLD provides a priority encoding function of the four match flags that are brought out in parallel. In the cycle following the compare, the /ELOCK signal is brought LOW to ensure that only the highest-priority CAM responds for Status Register reads or operations on the highest match. If there is no system match and a TCO CT, for example, is needed to change the mask register for all devices, the /ELOCK signal would be kept high in the subsequent cycle so that the TCO CT instruction is broadcast to all the devices.

In this approach, the /EC signal is tied high on all MU9C1485A/Ls to disable the match daisy chain. As such, the /MF flag is no longer active and is left disconnected. The Full flag daisy chain is still utilized in its normal configuration with the /FF output from one device input to the /FI pin on the next device in the daisy chain.

Although only four devices are shown in the example, the approach can easily be expanded to work with more MU9C1485A/Ls by using larger PLDs. This approach can also be subsumed into the ASIC that contains the state machine controlling the MU9C1485A/Ls.

An external priority encoder is also useful because it develops a system match flag more quickly than the daisy chain approach. Additionally, the system match flag timing will be independent of the number of CAMs installed. The following example compares timing for daisy chain configurations against the PLD approach. This example assumes -90 MU9C1485A/Ls driven by a 40 MHz clock, but the concept can be readily applied to other configurations.

In daisy chained systems, installation of additional CAM devices will result in additional delay to when the system match flag is valid. Timing for daisy chains of 4, 8 and 16 CAMs is given in Figure 4. As can be seen, with more devices in the daisy chain, the /E HIGH period will need to be lengthened. In this particular example, /E is kept high anywhere from three to six clock cycles to allow the daisy chain to settle.

By using an external priority encoder, just a single PLD propagation delay is required to resolve the highest-priority matching CAM. This is illustrated in Figure 5. Quick resolution of the highest-priority CAM allows a subsequent CAM cycle to be started in just two cycles of the clock, resulting in an overall performance improvement.

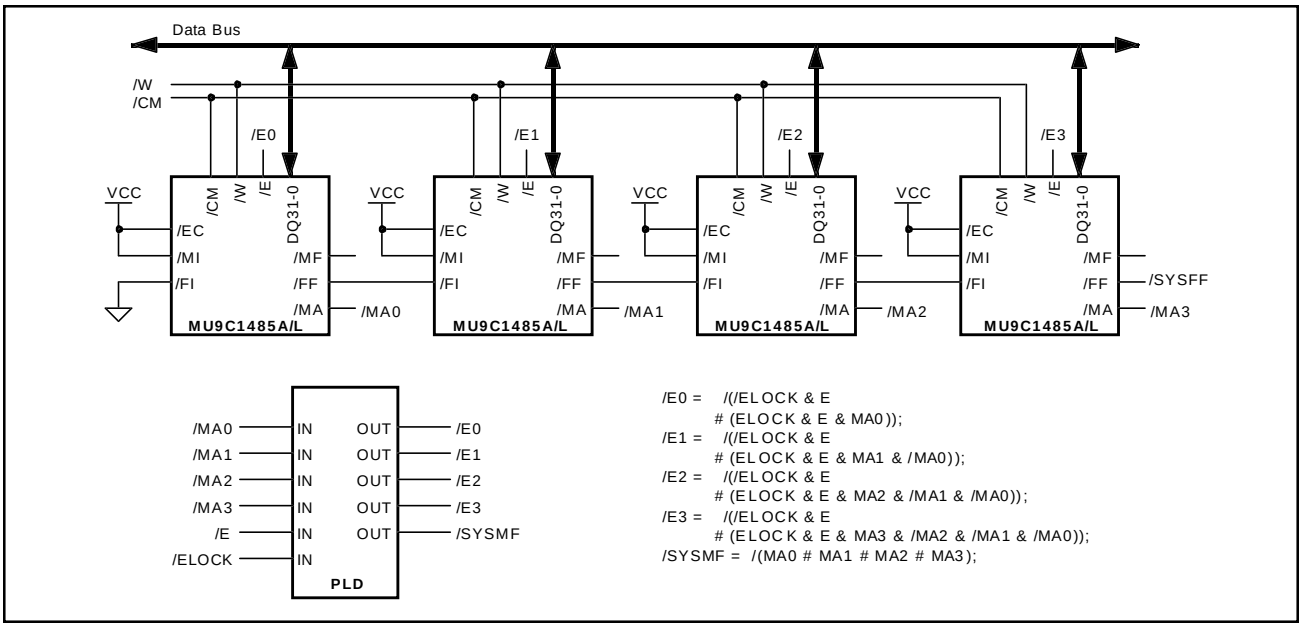


Figure 3: External Priority Encoder

EXAMPLE ETHERNET CODE SEQUENCES

Initialization and Configuration of the CAM Database

The Initialization and Configuration routine is constructed to configure four MU9C1485A/L WidePort LANCAMs for use with the following filter and table management routines (note that the indicated /E = H timings will support up to five 70ns devices). Lines 1 through 11 initialize the LANCAMs. Line 1 clears up any power-up anomalies that may be left in the part. Line 2 sets all devices to listen to the following commands. Line 3 resets the devices.

Lines 4 through 10 give a unique Page address to each CAM in the chain. Line 4 targets the Page Address register of the highest-priority (lowest address value) device in the chain and sets the Page Address value. Line 5 sets the Full flag on this device, forcing the next device in the chain to respond to the next set of initialization commands. This cycle of targeting the Page Address register, setting the Page Address value, and setting the Full flag is repeated until all devices in the chain have a unique Page Address value. Line 11 resets all devices, returning the Full flags to their normal function.

Lines 12 through 19 configure the Background Register set for use in the Purge on Time Stamp, Set Address Register, and Read Entries routines. Line 13 configures the CAMs as 64 bits CAM, 0 bits RAM, and Mask Register 1 for compares. The Address register is configured to auto-increment. Lines 14 to 16 initialize Mask Register 1 for use in comparing on only the Time Stamp and Permanent bits. Line 17 sets the Segment Control register to write to Segment 0 (Permanent bit, Port ID, Time Stamp), and read Segments 0 and 1. Line 18 sets the Persistent destination for Data writes to the Comparand register. Line 19 sets the Persistent source for Data reads to Memory at Address register (the memory location the Address register is pointing to).

Lines 20 through 27 configure the Foreground Register set for the DA and SA filtering operations, and the addition and deletion of permanent entries. Line 21 configures the CAMs as 48 bits CAM, 16 bits RAM, no mask register for compares, and sets the response mode to Enhanced. Line

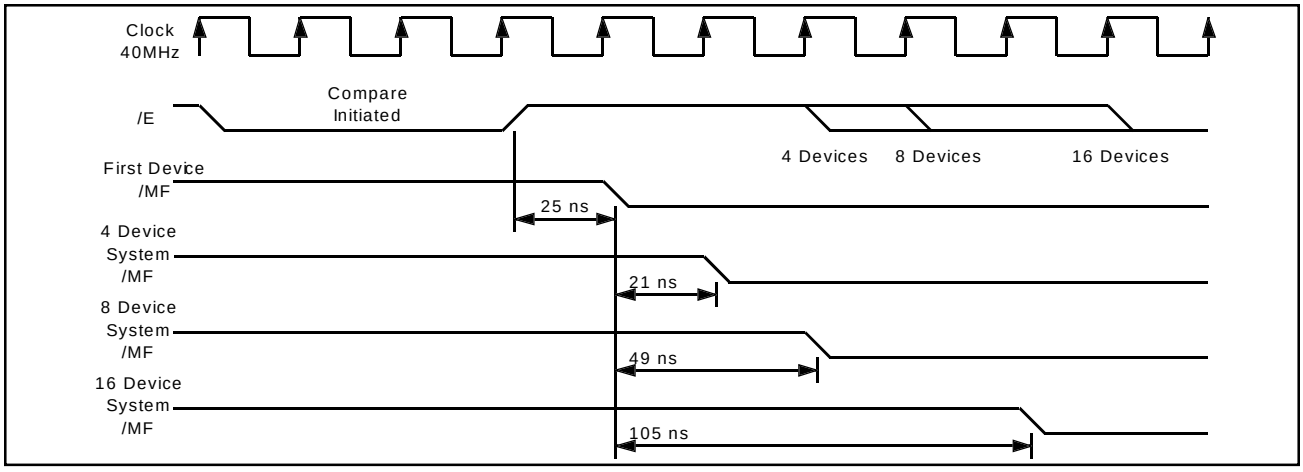


Figure 4: Daisy Chain Timing for 4, 8, and 16 CAMs

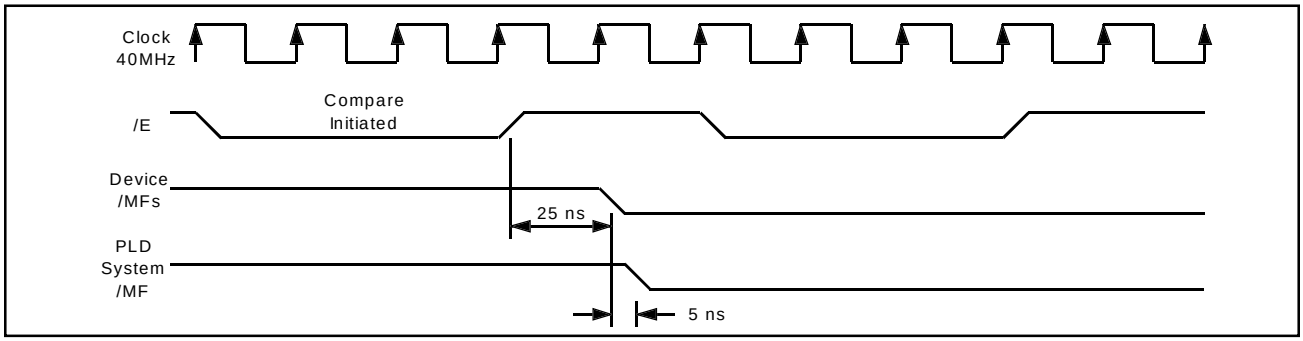
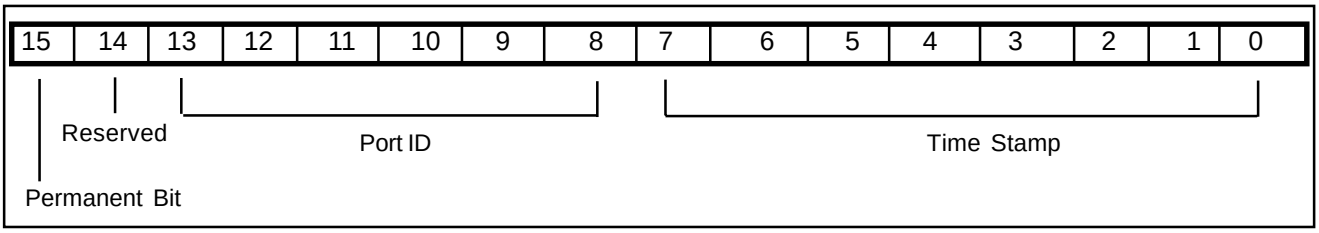


Figure 5: External Priority Encoder Timing



Associated Data Field (Lowest 16 bits) Bit Assignments

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	L	H	20	20	H		0000 0000	Command Read Clears Power-up anomalies
2	L	L	20	20	H	TCOW_DS	0A28 FFFF	Target Device Select register Select all devices
3	L	L	40	20	H	TCOW_CT	0A00 0000	Target Control register Reset all devices
4	L	L	20	20	H	TCOW_PA	0A08 0000	Target Page Address register Set Page address = 0 for first device
5	L	L	60	20	H	SFF	0700 0000	Set Full flag
6	L	L	20	20	H	TCOW_PA	0A08 0001	Target Page Address register Set Page address = 1 for second device
7	L	L	60	20	H	SFF	0700 0000	Set Full flag
8	L	L	20	20	H	TCOW_PA	0A08 0002	Target Page Address register Set Page address = 2 for third device
9	L	L	60	20	H	SFF	0700 0000	Set Full flag
10	L	L	20	20	H	TCOW_PA	0A08 0003	Target Page Address register Set Page address = 3 for fourth device
11	L	L	40	20	H	TCOW_CT	0A00 0000	Target Control register Resets Full flag in all devices
12	L	L	20	20	H	SBR	0619 0000	Select Background Register set
13	L	L	20	20	H	TCOW_CT	0A00 8011	Target Control register 64 CAM,0 RAM,MR1,Enhanced Mode, Incr AR
14	L	L	20	20	H	SPD_MR1	0108 0000	Set Persistent destination to MR1
15	H	L	20	20	H		FFFF 7F00	Bits 31–16 : Opaque mask Bits 15–0 : Time Stamp and Perm bit only
16	H	L	20	20	H		FFFF FFFF	Bits 31–0 : Opaque mask
17	L	L	20	20	H	TCOW_SC	0A10 0040	Target Segment Control register Write segment 0, Read segments 0:1
18	L	L	20	20	H	SPD_CR	0100 0000	Set Persistent destination to Comparand
19	L	L	20	20	H	SPS_M@[AR]	0004 0000	Set Persistent source to Memory @ AR
20	L	L	20	20	H	SFR	0618 0000	Select Foreground Register set
21	L	L	20	20	H	TCOW_CT	0A00 8041	Set Control register 48 CAM,16 RAM, No Mask, Enhanced M, Incr AR
22	L	L	20	20	H	TCOW_SC	0A10 0800	Set Segment Control register Write Segments 0:1, Read Segment 0
23	L	L	20	20	H	SPD_MR1	0108 0000	Set Persistent destination to MR1
24	H	L	20	20	H		0000 8000	Bits 31–16 : Transparent mask Bits 15–0 : Mask Permanent bit only
25	H	L	20	20	H		0000 0000	Bits 31–0 : Transparent mask
26	L	L	20	20	H	SPD_CR	0100 0000	Set Persistent destination to Comparand
27	L	L	20	20	H	SPS_M@HM	0005 0000	Set Persistent source to Highest match

Initialization and Configuration Routine

NOTES:

1. xxxx = “Don’t Care”
2. dddd = Data Value written to or read from the CAM database
3. aaaa = Memory location of CAM you want to read from
4. pppp = Page Address value of the device to be read from

22 sets the Segment Control register to write to Segments 0 to 1, and read from Segment 0. Lines 23 to 25 initialize Mask Register 1, which is used during the update operation of the SA Filter routine. Line 26 sets the Persistent destination to the Comparand register, and Line 27 sets the Persistent source to the Highest match (highest-priority matching memory location's Associated data).

The CAM database has been configured to have the lowest 16 bits of the 64-bit entry contain the Associated Data field, which is the Time Stamp, Port ID, and Permanent bit. The remaining bits (bits 63–16) contain the 48-bit Ethernet address. The mask registers in both the Foreground Register set and Background Register set have been configured to have the following Associated Data Field Bit assignments: 8 bits of Time Stamp to support a resolution of 1-of-256, 6 bits of Port ID to support up to 64 ports, and the Permanent Bit feature to support addresses that do not get aged out. These bit assignments are shown in the table on page 7.

Address Filter Routines

The Destination Address Filter routine is the highest-priority routine, followed closely by the Source Address Filter routine. Each of these routines may need to be run up to 12 times per arbitration cycle (once for each of 12 ports), which implies that under the worst-case conditions of all 12 ports receiving a minimum size packet at the same time, the associated data from the DA filter routine will be available for the last port after 2.64µs. One of the management routines can be run once per arbitration cycle, since these routines are far less time critical.

The Match flag is available by the end of the data cycle on Line 2. The associated data is read to get the Port ID of the matching entry. If the Port ID is the same as the port initiating the DA routine, the port should be signaled to reject the frame (assuming negative filtering).

Note that the SA Filter routine requires a decision to be made in the state machine, based on whether or not a match exists. If a match is found, line 3a updates the Time Stamp and Port ID are updated by moving the contents of the Comparand register through MR1 to the location of the highest priority match in the CAM. If a match is not found, line 3b learns the new address, along with its Port ID and the current Time Stamp by moving the contents of the Comparand register to the Next Free memory location. Also note that the Permanent bit is always 0, ensuring that any Source address learned by this routine can be purged if it becomes inactive.

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	H	L	20	20	H		dddd xxxx	Write lowest 16 bits of addr. to bits 31–16 Dummy write to bits 15–0
2	H	L	60	40	L		dddd dddd	Write highest 32 bits of addr. to bits 31–0 and compare
3	H	H	60	20	H		xxxx ddxx	Read Associated data, Port ID on bits 13–8 FFFF FFFF on bits 31–0 if no match

DA Filter Routine - Total Time=220ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	H	L	20	20	H		dddd dddd	Write lowest 16 of addr. bits to bits 31–16 Write Perm Bit, Port ID and TS to bits 15–0
2	H	L	60	40	L		dddd dddd	Write highest 32 bits of addr. to bits 31–0 and compare
If a match is found, Update Time Stamp & Port ID								
3a	L	L	60	20	H	MOV_HM, CR, MR1	0368 0000	Move to Highest match through MR1 to Update Time Stamp and Port ID
If no match is found, Learn new address								
3b	L	L	60	20	H	MOV_NF, CR,V	0334 0000	Moves SA to Next Free w/ Time Stamp and Port ID

SA Filter Routine - Total Time=220ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	L	L	20	20	H	SBR	0619 0000	Select Background Register set
2	H	L	60	20	H		xxxx 00dd	Load Time Stamp value to purge and compare
3	L	L	60	20	H	VBC_ALM,E	043D 0000	Mark all matching entries “Empty”
4	L	L	20	20	H	SFR	0618 0000	Select Foreground Register set

Purge on Time Stamp - Total Time=240ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	H	L	20	20	H		dddd ddxx	Write lowest 16 bits of addr. to bits 31–16 Write Perm Bit and Port ID to bits 15–8
2	H	L	20	20	H		dddd dddd	Write highest 32 bits of addr. to bits 31–0
3	L	L	60	20	H	MOV_NF, CR,V	0334 0000	Move to Next Free

Add a Permanent Entry - Total Time=160ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0]	Description
1	H	L	20	20	H		dddd xxxx	Write lowest 16 bits of addr. to bits 31–16 Dummy Write to bits 15–0
2	H	L	60	40	L		dddd dddd	Write highest 32 bits of addr. to bits 31–0 and compare
3	L	L	60	20	H	VBC_HM,E	042D 0000	Set Highest match to “Empty”

Delete an Entry - Total Time=220ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31-0] (HEX)	Description
1	L	L	20	20	H	SBR	0619 0000	Select Background Register set
2	L	L	20	20	H	TCOW_AR	0A20 aaaa	Target Address register on bits 31–16 Address value on bits 15–0
3	L	L	20	20	H	SFR	0618 0000	Select Foreground Register set

Set Address Register - Total Time=120ns

	/CM	/W	/E=L (ns)	/E=H (ns)	/EC	Mnemonic	DQ[31–0] (HEX)	Description
1	L	L	20	20	H	SBR	0619 0000	Select Background Register set
2	L	L	20	20	H	TCOW_DS	0A28 pppp	Target Device Select register on bits 31–16 Page Address value on bits 15–0
3	H	H	60	20	H		dddd dddd	Data Read, Lower 32 bits
4	H	H	60	20	H		dddd dddd	Data Read, Upper 32 bits
5	L	H	40	20	H		dddd dddd	Command Read, Status register
6	L	L	20	20	H	TCOW_DS	0A28 FFFF	Target Device Select register on bits 31–16 Select all devices on bits 15–0
7	L	L	20	20	H	SFR	0618 0000	Select Foreground Register set

Read Entries - Total Time=380ns

Table Management Routines

The following table management routines are low priority routines. One of these routines may be run per arbitration cycle, with the Purge on Time Stamp routine being the highest-priority management routine. Adding a permanent entry, deleting an entry, or reading the contents of the CAM database are not time critical. The system performance will not be impacted if these routines are held off for a few arbitration cycles.

EXAMPLE ATM CODE SEQUENCES

ATM Initialization Code

The initialization code for an ATM application is similar to that given for an Ethernet application. The main differences are in the Segment Control register setting, only 32 bits of comparand data need to be loaded, and in the Mask register settings, the ATM header is shorter than the 48-bit addresses used in Ethernet. The Segment Control register is set up to load the 32-bit ATM header into Segment 1 of the CAM's Comparand register. Once loaded a comparison is executed to identify the incoming ATM cell. Mask Register 1 in the Foreground register is used on comparisons that search for Virtual Channel Connection (VCC) comparisons, allowing both the VPI and VCI fields to participate in the comparison. Mask Register 1 in the Background register is used for Virtual Path connection (VPC). It allows only the VPI bits to be significant in the comparison. Note that it is possible to just use a single Mask register if "don't care" bits from the ATM header are always set to a consistent state. As such, no Mask register would be needed for the comparison of the full VPI and VCI fields, and the single Mask register would be used to perform a Virtual Path comparison, masking the VCI field of the header. Another optional configuration could perform Virtual Path compares in parallel in a separate RAM for improved throughput.

Lookup ATM Connection Code

Upon arrival of an ATM cell, the VPI and VCI are extracted from the cell header and written into the Comparand register, as shown in Table 13. Writing to the Comparand register will initiate an automatic comparison cycle utilizing MR1 in the Foreground register. In the event of a match, the Status register is read to obtain the address of the matching entry. This address may then be used to lookup data associated with the particular connection in external memory. If the compare with MR1 does not find a full VPI/VCI match, a subsequent write to the control register is used to change to the Background Register set. This write to the Control register automatically initiates a comparison using the new selection of MR1, checking for a VPI-only match. After the comparison, the Status register is read to determine the matching address. A subsequent Command write of SFR is used to reselect the Foreground Register set MR1 for comparisons. Alternatively, additional performance can be gained by not selecting the Foreground Register set and just starting off with the comparison using MR1 of the Background Register set when the next ATM cell arrives. In this case, a little more complexity is added to the control hardware for keeping track of the match looking for a VPC and the match looking for a VCC.

Note that the associated data for a particular connection could be stored in Segment 0 of the CAM if it were limited to just 32 bits in width. Typically however, more than 32 bits of associated data are required in ATM, mandating an external RAM for the storage. Associated data may include such things as the translated VPI/VCI, internal switch routing information, internal switch headers, as well as billing and traffic parameters.

Entries associated with Virtual paths can be put into a small external RAM, resulting in a significant performance improvement. As seen in Table 14 on page 12, only a single comparison for a Virtual channel is now required. This is followed by a single status read to find the address of the associated data in external memory.

Add ATM Connection Code

New connections may be added to the CAM database by writing the appropriate header to the Comparand register and then moving it to the Next-Free address in memory, shown in Table 15 on page 12. A subsequent comparison on the header data can be used to obtain the address where the new connection was added. (Care should be taken to ensure that MR1 is selected when performing this operation.) Once the address is found, it can be used to add associated data into an external RAM.

Delete ATM Connection Code

The method for deleting a connection from memory is shown in Table 16 on page 12. The first step is to load the connection's header into the Comparand register. This will initiate an automatic compare cycle, identifying the location of the entry in the database. This entry may then be deleted using the Validity Bit Control instruction, setting the validity of the entry to Empty. Note that MR1 should be the selected comparison mask when deleting Virtual channels. MR1 may also be used when deleting Virtual paths if the VCI bits are set to a known state. If the location of the entry in memory is needed, a read may be performed prior to the VBC instruction. This can be useful if the external associated data needs to be accessed one last time to properly terminate the connection.

Condition	Cycle	Mnemonic & Value	DQ31-16	DQ15-0	/EC	tELEH
	CW	TCO DS, FFFFH	0A28	FFFF	HI	Short
	CW	TCO CT, 0000H	0A00	0000	HI	Medium
Repeat, inc “n”	CW	TCO PA, 000nH	0A08	000n	HI	Short
For all devices	CW	SFF	0700	0000	HI	Long
	CW	TCO CT, 0000H	0A00	0000	HI	Medium
	CW	SBR	0619	0000	HI	Short
	CW	TCO CT, 8091	0A00	8091	HI	Long
	CW	SPD MR1	0108	0000	HI	Short
	DW	FFFF,FFFH	FFFF	FFFF	HI	Short
	DW	0000F, FFFH	000F	FFFF	HI	Long
	CW	TCO SC, 2808H	0A10	2808	HI	Short
	CW	SPS CR	0100	0000	HI	Short
	CW	SPS M@HM	0005	0000	HI	Short
	CW	SFR	0618	0000	HI	Short
	CW	TCO CT, 8091H	0A00	8091	HI	Long
	CW	SPD MR1	0108	0000	HI	Short
	DW	FFFFH, FFFFH	FFFF	FFFF	HI	Short
	DW	0000H, 000FH	0000	000F	HI	Long
	CW	TCO SC, 2808H	0A10	2808	HI	Short
	CW	SPD CR	0100	0000	HI	Short
	CW	SPS M@HM	0005	0000	HI	Short

Table 12: MU9C1485A/L ATM Initialization Code

Condition	Cycle	Mnemonic & Value	DQ31-16	DQ15-0	/EC	tELEH
	DW	ATM Header	header1	header0	LO	Long
/MF LOW	CR	Status	status1	status0	HI	Medium
/MF HIGH	CW	SBR	0619	0000	LO	Short
/MFHIGH	CR	Status	status1	status0	HI	Medium
/MFHIGH	CW	SFR	0618	0000	HI	Short

Table 13: MU9C1485A/L ATM VPC and VCC Header Lookup Code

Condition	Cycle	Mnemonic & Value	DQ31-16	DQ15-0	/EC	tELEH
	DW	ATM Header	header1	header1	LO	Long
	CR	Status	status1	status1	HI	Medium

Table 14: MU9C1485A/L ATM VCC Header Lookup Code

Condition	Cycle	Mnemonic & Value	DQ31-16	DQ15-0	/EC	tELEH
	DW	ATM Header	header1	header0	HI	Long
	DW	MOV NF,CR,V	0334	0000	HI	Medium
	CW	CMP V	0504	0000	LO	Long
	CR	Status	status1	status0	HI	Medium

Table 15: MU9C1485A/L Add ATM Connection Code

Condition	Cycle	Mnemonic & Value	DQ31-16	DQ15-0	/EC	tELEH
	DW	ATM Header	header1	header0	HI	Long
	DW	VBC ALM,E	042D	0000	HI	Medium

Table 16: MU9C1485A/L Delete ATM Connection Code

MUSIC Semiconductors Agent or Distributor:

MUSIC SEMICONDUCTORS

http://www.music-ic.com
email: info@music-ic.com

USA Headquarters
MUSIC Semiconductors
254 B Mountain Avenue
Hackettstown, New Jersey 07840
USA
Tel: 908/979-1010
Fax: 908/979-1035
USA Only: 800/933-1550 Tech. Support
888/226-6874 Product Info.

Asian Headquarters
MUSIC Semiconductors
Special Export Processing Zone 1
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 49 549 1480
Fax: +63 49 549 1023
Sales Tel/Fax: +632 723 62 15

European Headquarters
MUSIC Semiconductors
Torenstraat 28
6471 JX Eygelshoven
Netherlands
Tel: +31 45 5462177
Fax: +31 45 5463663