MUSIC SEMICONDUCTORS

APPLICATION NOTE AN - N1

ENHANCING LAN BRIDGE DESIGNS WITH ASSOCIATED DATA

by Steve Stas

1.0 GENERAL

The MUSIC Semiconductors MU9C1480 LANCAM is a 1024 x 64 Content-Addressable Memory device intended for LAN bridge and router address filtering applications. The device uses internal registers and logic circuitry controlled by a rich instruction set designed to minimize the external logic and local processor overhead necessary for control of the bridge and router functions. LAN bridges will increase performance and lower system cost by using several unique features of the LANCAM. This Application Note outlines some of these very powerful features. Refer to the MU9C1480 Handbook for more detail.

This device's data translation facility allows multi-port bridges to convert in real-time the bit order of IEEE 802.3 to and from IEEE 802.5 formats within the LANCAM without external translation logic. Since this feature is invoked by the Control register, using or not using this facility can be changed as needed. This flexibility may allow the LANCAM to be shared among dissimilar ports in a multi-port bridge system.

The CAM/RAM partitioning feature and the extra width (64 bits) of the device enable a system designer to store “Associated Data” with every CAM word to further increase system throughput by storing intelligence or flags applicable to each node address. Some of these uses of Associated data will occupy only a few bits of the available RAM sector, allowing implementation of multiple flags or functions. The CAM/RAM partitioning can be changed under the auspices of the Control register. Further, the memory word status bits allow any number of individual memory locations to be tagged “RAM only,” allowing creation of internal scratchpad locations to augment registers and logical operations.

2.0 SOME USES OF ASSOCIATED DATA

Aging Algorithm

An algorithm that “ages” all the nodes contained in the station list based on the time elapsed since each node was referenced, and purges the station list of all node addresses not active within a certain elapsed time interval can considerably reduce the depth of the CAM needed to store the station list. Some applications can achieve an order-of-magnitude decrease in the CAM space required by purging aged entries. This characteristic implies that a network requirement of 32K stations could be stored in only three LANCAMs by storing and maintaining only those node addresses with recent activity. Aging or access history information can be stored as Associated data with the station address.

Port Address and Other Data Storage

Multi-port bridges can be more efficiently implemented by storing port addresses or type codes as data associated with the station address. Access via the highest-priority match uses a simple Data Read cycle. Other application-specific information such as control or routing data or commands unique to specific nodes or groups can be encoded and stored as Associated data.

The MUSIC MU9C1480 LANCAM 64-bit word array can be partitioned as CAM/RAM on 16-bit boundaries by manipulating the Control register in real-time (e.g., 48 CAM bits and 16 RAM bits per location, 32/32, etc.). This feature creates the ability to store Associated data with each CAM (or associative) word in the array. Note that the RAM partition is the low-order segment in CAM/RAM.

Since LAN node addresses are 48 bits wide, a word partition of 48 CAM and 16 RAM allows 16 bits of Associated data to be stored in the same CAM location as the 48-bit node address, and to be accessed with the CAM contents as a function of node address searches. The Associated data can be accessed directly or utilized in a number of ways depending upon application requirements. It can be accessed during an address filtering routine immediately after a match occurs on the 48-bit CAM word by the use of the “Read Memory at Highest-priority Match” instruction, or it can be included as part of the CAM memory word to be matched against the Comparand register during a Compare operation. The Control register can be changed as needed to move the CAM/RAM boundary and “zoom” into the Associated data field for operations like selecting entries based on a port address, for example. Alternatively the Mask register can be loaded with a mask that allows a comparison on only the 16 bits of Associated data. A possible example would be a router or a multi-port bridge appending a port address to the 48-bit node address, and either forming a 64-bit address for comparison search, or comparing through a Mask register to distinguish port addresses.

3.0 ONE WAY TO “AGE” THE STATION LIST

There are a number of ways to “age” the station list; some make use of more bits of available memory, and some may require more local bridge processor action. At least one approach uses memory space very well and minimizes local processor overhead. The aging approach used depends upon application parameters and protocols. However, all can reduce the amount of CAM required to implement an effective bridge.

The LANCAM is assumed to be partitioned as 48 CAM bits and 16 RAM bits per word as part of the initialization procedure (see Figure 5). As the station list is learned by the bridge, and the CAM is loaded with the node addresses, or as a node address is accessed or “Hit,” Bit 0 of the 16-bit Associated data sector is set to “1,” denoting a recently accessed node. Arbitrarily, we assign this bit to be the history or “Hit” bit for this example; the remaining 15 bits are “don't care.” If Bit 0 contains a “0” for a given entry after an interval arbitrarily chosen to be the “aging” interval, that node has not been accessed during that interval and can be purged. For this example, 500 ms is the aging interval (this interval can vary as applications may demand).

The local bridge controller (referred to hereafter as the local processor) maintains an aging interval routine that polls the CAM every 500 milliseconds and searches for those locations that have not been hit during the interval. Those that have not been hit are purged by the simple expedient of setting the Validity bits to “empty” on those non-hit locations. The next local processor step is to reset the “Hit” bit in all “hit” locations to a “0” to await the expiration of the next aging interval. During that interval some locations will be “hit,” and their “Hit”

bits will be set to “1,” maintaining them in the list. At the end of the aging interval the local processor again searches for “Hit” bits still set to “0,” and sets the Validity bits at those locations to “empty.” The following operations comprise these purging and resetting routines:

Purge Routine (Figure 1)

1. The local processor issues a Temporary Command Override (TCO SC) to the LANCAM to set the Destination Segment counter to enable the loading of four segments, necessary to load a 64-bit word to Mask Register 1 (MR1) in the subsequent steps.

2. The local processor issues a Set Persistent Destination (SPD) instruction to the CAM to set the destination of the next Data Write to MR1 to load a mask that isolates the Hit bit.

3. The local processor writes a 64-bit word (four segments) using four Data Write cycles to MR1 masking all bits but the Hit bit.

4. The local processor issues another TCO SC instruction to set the Destination Segment counter back to the normal mode of loading three segments (count limits set to 01_B and 11_B) and to load 00_B into the Destination Segment counter, forcing the next write to the Comparand register to write to Segment 0, which contains the Associated data to be searched. The Segment Control register data is loaded on the next immediate Command Write cycle following the TCO SC (see the MUSIC MU9C1480 LANCAM Handbook for Segment Control register bit assignments).

5. The local processor issues a TCO instruction to set the Control register to perform a 64-bit compare through MR1 (TCO CT), followed by the appropriate immediate data on the next Command Write cycle.

6. The local processor issues an SPD instruction to return the persistent destination for data to the Comparand register (SPD CR).

7. The local processor writes a 16-bit word to the Comparand register having a “0” in the Hit bit location via a simple Data Write cycle (/CM is HIGH, and /W is LOW). The Compare function that follows is looking for locations that have not been “hit.”

8. The local processor issues an explicit compare instruction (CMP V). This is necessary because the Segment Counter end limit has not been reached. Note that an automatic compare will occurr only at the end of a cycle in which the Segment Counter end limit is reached. The Status register will now contain the match information in the Match bit and Multiple Match bit. All locations containing “0” in the Hit bit will be match responders.

9. The local processor issues a “Set Validity bits at all matching locations” instruction to set all matching locations (those with a “0” in the Hit bit have not been referenced during this interval) to “empty” (VBC ALM, E). This instruction will set all non-hit locations to empty in one cycle. The memory is now purged of non-hit entries.

10. The local processor issues a Temporary Command Override instruction in favor of the Control Register (TCO CT) to return the device to the normal state of 48-bit comparisons with 16-bit RAM fields. The next immediate Command Write cycle contains the Hex data value to be loaded into the Control Register.

11. The local processor issues a Move Memory to Comparand instruction (MOV CR, aaaH), to move the contents of the scratchpad location containing the proper polarity “Hit bit” to the Comparand Register, thereby storing the “Hit bit” in the comparand for immediate tagging when a match occurs. This function is described fully under the section entitled “Setting the Hit Bit.”

Reset Routine

All previously hit locations need to be flagged immediately for the next aging interval as non-hit, so they can be updated to “hit” as they are accessed by the system, and be tagged as “non-hit” for the expiration of the new interval if they are not. At first glance, it appears that all previously “hit” locations must be stepped through and their “Hit” bits reset to “0,” denoting “non-hit,” for the new interval. However, this time-consuming routine is not necessary if we utilize a programming trick in the local processor software logic. A far more efficient approach is to implement the seven steps of the purge routine as outlined above, but in lieu of the many steps that would be required to sequentially update the Hit bit for each location, simply toggle the local processor program logic to now consider a “1” as non-hit instead of “0.” By so doing, all locations are reset without executing the repetitive loop of a reset routine. The definition of the Hit bit polarity is clearly arbitrary, as long as the program logic keeps track. After every aging interval the local processor toggles its logic back and forth to consider a “1” then a “0” as a “hit.” This approach eliminates an additional reset routine. The toggle, which now defines a “0” as “Hit” is done by inverting the polarity of the Hit bit to be searched in step 5 of the purge routine, and by writing a “0” to the Hit bit in the Associated data of each node address as a new address is added to the CAM's contents. Also, the Hit bit is now written to the CAM Comparand register as a “1” rather than a “0”; the search is for all locations containing a “1” (now defined as “non-hit”). The toggle can be easily done by utilizing two locations of the LANCAM as data storage locations and simply moving the appropriate data value to be used for the Hit bit into the Comparand register, as described below.

Optimum Purge Routine (Figure 2)

The Purge routine may be made more efficient, depending upon local processor speed and application requirements, by using a few locations of the LANCAM as scatchpad storage for the different mask values and Hit bit polarities. At system initialization, several locations can be set to “RAM-only” by setting their Validity bits. These locations will not be included in any Compare operations when so tagged. During system initialization, rather than storing a mask in local processor system memory or registers, the local processor writes a mask to the selected “RAM-only” location in the LANCAM for the Hit bit isolation in MR1, a data value into another location for the purge when Hit=0, and another for use when Hit=1. Other locations can be tagged as “RAM-only” and used to store other mask or data values, and moved as needed to the Mask registers or the Comparand register.

In place of steps 1 through 4 of the above Purge Routine, the local processor issues a “Data Move to Mask Register 1 from Memory at Address” (MOV MR1, aaaH) instruction to the LANCAM, and provides the address of the location used as the scratchpad storage for the MR1 mask as immediate data in the next cycle after the instruction (two Command Write cycles). Steps 5 through 9 remain the same, except the SPD instruction in step 6 is no longer needed since the Comparand always remains the persistent destination. This approach reduces the first five LANCAM cycles to two cycles. The local processor can perform other system functions, and the LANCAM completes this background function more quickly, allowing it to return to the foreground task of address filtering. The choice of which approach to use is dictated by system speed and memory requirements.

Setting the Hit Bit

The procedure necessary to set the Hit bit in the first place, after a successful comparison has been made to tag a location as “hit,” is also important. The tagging of locations as “hit” is a foreground real-time operation since it occurs in every normal compare transaction when a node address is located as a result of address filtering. Consequently, the tagging operation must consume very few cycles of a Compare sequence or the whole aging concept fails since a bridge handling FDDI must complete its business in about 700 ns.

Several useful features of the LANCAM assist in accomplishing the tagging of “hit” locations. When the device is set to 48 CAM bits, only the upper 48 bits of the Comparand register participate in the comparison, while the lower 16 bits can act as a separate resource. The lower 16 bits of the Comparand register do not take part in the Compare operation; moreover, those lower 16 bits are also not disturbed by a three-cycle load of the other 48 bits of the Comparand register. As a result, any data stored in the first segment (lower 16 bits) of the Comparand register will remain until specifically changed by the user, and can be a further storage resource to implement logical operations, such as appending Associated data to an entry after Associative operations. This characteristic is designed to facilitate the use and manipulation of Associated data, one of the prime reasons to have the 64-bit width in the first place.

To minimize the number of cycles required to match a node address in the address filter function, and tag each “hit” location to age it, our approach uses the first segment of the Comparand register to pre-store the Hit bit value of correct polarity in order to tag each “hit” location as it is accessed by a true comparison. During initialization, a MOV CR, aaaH (Move to Comparand from Memory at Address) instruction is performed; aaaH is the address of the scratchpad location containing the data with the proper bit location set to the value that denotes a “hit.” The Comparand register will now contain a valid “Hit” bit to be stored back into each location as it is hit. As the Comparand register is loaded with the 48-bit node address to be searched, the lower 16 bits will be unchanged because the device is set to 48-bit (three-segment) loads by the state of the Control register as was done in step 10 of the initialization sequence. This condition persists, so the proper Hit bit value remains in the lower 16 bits of the Comparand register until changed by the local processor to reflect the inverted value after the software logic toggle. After the aging interval and the toggle, the correct Hit bit value is loaded via a MOV CR aaaH instruction. Note that if the newly toggled Hit bit polarity is loaded first, it can be used to test for the “missed” entries of the previous aging interval as part of the Purge routine and then used again to act as the “Hit” value to be appended to entries that are active in the current interval. This approach saves doing an extra MOVE operation at the boundary between aging intervals.

4.0 NORMAL ADDRESS FILTERING SEQUENCE

Figure 3, “Typical Address Filtering Sequence,” illustrates the code required to effect a compare and “hit” tag during a typical address filtering sequence. The foreground operation of the device is to receive 48-bit words for LAN address filter functions. The following steps are those required to load and compare node address data, and set the Hit bit to its proper value:

1. Write data to the Comparand register (three Data Write cycles):

    a. A Data Write from the Data bus of the first 16-bit segment of the 48-bit address to be tested (either the Source or the Destination address).

    b. A Data Write of the second 16-bit segment.

    c. A Data Write of the third 16-bit segment of the 48-bit word. The hardware Match flag, /MF, will be asserted at the end of this cycle if a match occurs, and if /EC is LOW at the start of that third cycle. Many applications will use only this hardware flag to ascertain a match, and skip the next cycle where the Status register is read to obtain the match condition.

2. Read the Status register using a Command Read cycle to determine if a match occurred. The “Read Status register” operation is the default case of a Command Read cycle; no instruction is required.

3. If a match occurred, the local processor issues a MOV HM, CR (Move Comparand to Highest-priority Match Location) instruction to the MU9C1480, which moves the contents of the Comparand register to the match location, and changes the Hit bit at that location to the proper value for “hit” because the Hit bit is stored in the lower 16 bits of the Comparand register. The initialization sequence, described in Section 6.0, will have stored the proper Hit bit value in the Comparand register's first segment. Alternatively, this Move operation can be done through the mask that isolates the Hit bit so that no other Associated data bits need be comprehended.

5.0 LEARNING THE NETWORK

When first turned on or when retrieving purged entries, the Bridge must learn node addresses from the Source address field in a given packet. If a search is unsuccessful, which implies that a node previously off-line is now on-line, that Source address must be added to the station list. The aging philosophy described by this application note will obviously generate some “learn” requirements, since stations may be purged repeatedly. This function can be implemented in real-time expediently by the use of a NOP followed by a MOV NF, CR, V (Move Data from Comparand Register to the Next Free Memory Address) instruction in lieu of the above MOV HM, CR (Move Comparand to Highest Priority Matched Location) instruction. This switch of instructions can be triggered when the local processor detects a “no match” condition by finding the /MF pin false at the appropriate point in the cycle. Since this instruction also stores the entire Comparand to a memory location, the tagging of the location as “hit” also takes place by virtue of the same characteristics described above. This sequence of instructions is shown in Figure 4. In systems where the LANCAM may be full, the Full flag (/FF) should be tested at the same time as the /MF pin. These can be done in parallel since each is likely to be connected to the Local processor's I/O bus.

6.0 INITIALIZATION SEQUENCE

The LANCAM must be initialized to perform its functions. If the above approach is used to dedicate MU9C1480 locations as scratchpad memory for masks and data storage, those locations must have “RAM-only” status. The following is a description of the initialization routine. The code steps are enumerated in Figure 5, “Example System Initialization Routine.”

1. To enable global access of the MU9C1480 array (the normal condition), the Device Select registers of all devices in a daisy chain must contain FFFFH otherwise each MU9C1480 will respond only to operations on the Data bus when its Page Address register matches the Device Select register. A TCO DS (Temporary Command Override, Device Select register - two Command Write cycles) is issued with FFFFH in the immediate data field to enable global access. If the application later requires it, access to a specific MU9C1480 device can be done by broadcasting a TCO DS instruction with the Page Address value of the desired device as the immediate data field. Only the device whose Page Address and Device Select registers match will be accessed on subsequent instructions, eliminating the need for external decoding. In a single LANCAM implementation, setting DS=PA will ensure access to the device under all conditions.

2. A TCO CT (Temporary Command Override, Control register) is issued with an immediate data field on the next Command Write cycle of 0000H to reset the MU9C1480 memory to all empty, and set the registers to their initial conditions. See the MUSIC MU9C1480 LANCAM Handbook for the details of the Reset operation. The default power-up condition is the same, but we assume here that a software reset is necessary so that the routine is universal.

3. The Page Address register is accessed via a TCO PA (Temporary Command Override, Page Address register - two Command Write cycles) to set each MU9C1480 to a unique Page address if multiple LANCAMs are vertically cascaded. The

immediate data field contains the desired Page address.

4. After each TCO PA, the SFF instruction (Set Full Flag - one Command Write cycle) is executed, which sets the Full flag of the previously accessed MU9C1480, causing the next MU9C1480 in the chain to respond to the next TCO PA, allowing its Page Address register to be loaded.

These two instructions are repeated for each successive LANCAM in the daisy chain. If only one MU9C1480 is used, these instructions may be skipped.

5. Another TCO CT (Temporary Command Override, Control register—two command Write cycles) is issued to reset all the Full flags to "not full." The Page Address registers in all of the devices in the chain are unaffected by this Reset operation.

6. A TCO CT is now issued to set the Control register to the desired system configuration. The immediate data field contains the value to be loaded into the Control register to effect this configuration. In the example of Figure 5, a value of 8040H is loaded, which results in the Match flag enabled, Full flag enabled, input not translated, memory configured as 48 bits CAM, 16 bits RAM, comparison through Mask registers disabled, and automatic address incrementing enabled (this last only applies to Read and Write to Memory at Address Register cycles).

7. Next, the Destination Segment counter must be set to allow 64-bit writes (four segments) to the array in order to load the appropriate data values to several MU9C1480 locations used as scratchpad for this purpose. To illustrate the general condition, this example assumes that several locations will be used as a scratchpad area.

   A TCO SC (Temporary Command Override, Segment Control register—two command Write cycles) is issued to set the Destination Segment counter to allow four segments to be loaded from the Data bus. The immediate field contains the appropriate value to cause this configuration. This example translates to 18C0H (see the MUSIC MU9C1480 LANCAM Handbook for details of the bit assignments in the Segment Control register), which loads the Destination Segment counter with binary 00, sets the Destination Segment counter to start at 00 and end at a count of 11, loads the Source Segment counter with 00, and sets the Source Segment counter to start at 00 and end at 11. The Source Segment counter is set the same as the Destination Segment counter for the time being. This is the default setting after a RESET.

8. The Address register is now set to the starting value of the desired scratchpad area with a TCO AR (Temporary Command Override, Address Register—two Command Write cycles); the immediate field contains the desired address. For clarity, we assume an address of 000H for this example. This is also the default setting after a RESET.

9. To load the scratchpad area, an SPD M@[AR], R instruction is executed (Set Persistent Destination, Memory Relative to Address Register, Set Location Status Bits to RAM-only). Note that this instruction also causes each location to be tagged as "RAM—only" as each location is written by the ensuing cycles. Address register auto-increment was set by the initialization of the Control register in step 6.

10. The first 64-bit data value is now loaded to location 000H of the device by the following four Data Write cycles. The Destination Segment counter rolls over, and the Address register increments, allowing the next 64-bit word to be directly loaded as four data writes immediately following the first four data writes with no further setup. Groups of four data writes can now fill and tag as "RAM-only" as many locations as are required for scratchpad by the application. A "hit bit" can be stored in Segment 0 of location 001H for this example.

11. The Segment Control register is now reconfigured to set the Destination Segment counter to do three-segment writes to handle the normal application address filtering requirement of 48-bit words. A TCO SC instruction is issued to set the Destination Segment counter limits to binary 01 start, and binary 11 stop. This example translates to 3808H as the immediate data field. The Source Segment counter starts at binary 00 and stops at binary 00, so that the 16-bit Associated data segment can be read in one cycle. The limits can, of course, be changed.

12. Since the persistent destination was the memory array, the Comparand register must become the persistent destination for the ensuing Compare operations of the application via an SPD CR (Set Persistent Destination, Comparand register) instruction. An SPD CR (or an SPS CR) must be issued only after a resource other than the Comparand register is set as a persistent destination or source.

13. In order to tag each "hit" location to age it when a true comparison occurs, Segment 0 of the Comparand register is loaded with the Hit bit value. A MOV CR, aaaH (Move to Comparand from Memory at Address) is executed; the immediate field is the address of the scratchpad location (001H) containing the proper value denoting "hit" in the Hit bit location. The Comparand register is now loaded with a valid Hit bit to be stored back into each location as it is accessed or hit. The MU9C1480 is now initialized for the application to load data to the Comparand register for filtering or learning functions.

14. To facilitate a one-cycle read of the 16-bit Associated data field, an SPS M@HM (Set Persistent Source, Memory at Highest Priority Match) command is issued to configure the persistent read. The previous setting in step 11 of the Source Segment counter to start and stop at binary 00 enables the persistent read of this segment in only one Data Read cycle.

7.0 OTHER POSSIBILITIES

Adding other concurrent Associative memory operations, such as appending port addresses to the basic node address, can also be done. The powerful functions of the MU9C1480, such as the second Mask register and the assignment of scratchpad memory areas, enable the performance of additional masking operations. For example, comparisons through a second mask isolating port addresses in the 16-bit Associated data memory sector, or 64-bit comparisons including a port address, but masking the Hit bit, can be implemented using the flexible MU9C1480 instruction set.

Figure 1: An Example Address Purge Routine

Assumptions: This routine loads Mask registers from the local processor rather than using LANCAM memory as scratchpad. Section 3 of this note gives a verbal description of this routine called the "Purge Routine."

Cycle Type	Opcode or Data on Data Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Command Write	TCO SC	L	L	L	H	Target segment counter to set count limits for four segments	
Command Write	1C04H	L	L	L	H	Segment counter immediate field to set (start = binary 00, end = binary 11, Dest. counter = 0)	
Command Write	SPD MR1	L	L	L	H	Set MR1 as destination for Data Writes	
Data Write	xxxxH	L	H	L	H	Load MR1 mask Segment 0 (value depends on Hit bit location	
Data Write	FFFFH	L	H	L	H	Load MR1 mask Segment 1	
Data Write	FFFFH	L	H	L	H	Load MR1 mask Segment 2	
Data Write	FFFFH	L	H	L	H	Load MR1 mask Segment 3	
Command Write	TCO SC	L	L	L	H	Target Segment counter to load a count of 00B and set count limits to 01B and 11B	
Command Write	3800H	L	L	L	H	Immediate field to load value	
Command Write	TCO CT	L	L	L	H	Set Control register for 64-bit compare thru MR1 to identify non-hits	
Command Write	FE1FH	L	L	L	H	Immediate field to load CT	3
Command Write	SPD CR[MR1]	L	L	L	H	Set Comparand register as destination thru MR1	
Data Write	xxxxH	L	H	L	H	Load Comparand Segment 0 with 16-bit word containing "Hit" bit of polarity indicating "no hit"	
Command Write	CMP V	L	L	L	H	Explicit Compare	
Command Write	VBC ALM,E	L	L	L	H	Clear all non-hits	1
Command Write	TCO CT	L	L	L	H	Set Control register for 48-bit compare with no mask	4
Command Write	FE4FH	L	L	L	H	Immediate field to load CT	
Command Write	MOV CR, aaaH	L	L	L	H	Target Comparand for move from scratchpad location with proper Hit bit polarity in Segment 0	2
Command Write	aaaH	L	L	L	H	Address of scratchpad location with Hit-bit value	2

Notes:

1. VBC instruction can follow Compare directly without status read, if matches occur, the VBC ALM, E command will reset all matching locations; if no match occurs, the VBC behaves as a no-op.
2. Send Hit bit in associated data field to Comparand from the scratchpad location containing the proper polarity, enabling efficient tag when compare is true. The logic of this function is described in Section 3.0 of this Application Note.
3. The Control register bit assignments are FE1FH for this example, see the MUSIC MU9C1480 LANCAM Handbook for detail.
4. The Control register bit assignments are FE4FH for this example, see the MUSIC MU9C1480 LANCAM Handbook for detail.

Figure 2: Optimum Purge Routine

Assumptions: This routine assumes that the user wishes to use the MU9C1480 LANCAM locations as RAM-only scratchpad to store masks, rather than deliver them from the local processor each time.

Cycle Type	Opcode or Data on Data Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Command Write	MOV MR1, aaaH	L	L	L	H	Move mask to MR1 from memory	
Command Write	0000H	L	L	L	H	Mask 1 address in scratchpad section	
Command Write	TCO SC	L	L	L	H	Target Segment counter to load count value = 00B	
Command Write	3800H	L	L	L	H	Immediate field to load Segment 0 value (binary 00 in Destination Segment counter)	
Command Write	TCO CT	L	L	L	H	Set Control register for 64-bit compare thru MR1 to identify non-hits	
Command Write	FE1FH	L	L	L	H	Immediate field to load CT	2
Data Write	xxxxH	L	H	L	H	Load Comparand Segment 0 with 16 bit word containing Hit bit of proper polarity to flag "non-hits"	
Command Write	CMP V	L	L	L	H	Explicit Compare	
Command Write	VBC ALM, E	L	L	L	H	Clear all non-hits	
Command Write	TCO CT	L	L	L	H	Set Control register for normal 48-bit compare without mask	
Command Write	FE4FH	L	L	L	H	Immediate field to load CT	3
Command Write	MOV CR, aaaH	L	L	L	H	Target Comparand for move from scratchpad location containing proper Hit bit polarity in Segment 0	1
Command Write	aaaH	L	L	L	H	Address of scratchpad location with Comparand value with proper Hit bit	1

Figure 2: Optimum Purge Routine (Cont'd)

Notes:

1. Send Hit bit in Associated data field to Comparand from the scratchpad location containing the proper polarity, enabling efficient tag when compare is true. Location 000H contains value with "Hit" = 1. The logic of this function is described in Section 3 of this note.
2. The Control register bit assignments are FE1FH. For this example, see the MUSIC MU9C1480 LANCAM Handbook for detail.
3. The Control register bit assignments are FE4FH. For this example, see the MUSIC MU9C1480 LANCAM Handbook for detail.

Figure 3: Typical Address Filtering Code Sequence with List Aging Function

Assumptions: The "Hit" bit is to be set in the Associated data field (Segment 0) after each match.

Destination Segment counter limits have been set to start = 01, end = 11 for a 48-bit load as in initialization and purge routine examples.

The first segment of the Comparand register has been pre-loaded during the initialization routine with the appropriate mask containing the Hit bit of proper polarity, and any other bits of the Associated data field (Segment 0), if used, are preset to the desired values by the application, as shown in other examples.

Cycle Type	Opcode or Data on Data Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Data Write	xxxxH	L	H	L	H	Input from local bus, to Segment 1	1
Data Write	xxxxH	L	H	L	H	Input from local bus, to Segment 2	
Data Write	xxxxH	L	H	L	L	Input from local bus, to Segment 3	2
Command Read	Status	L	L	H	L	Output to data bus from Status register	3
Command Write	MOV HM, CR	L	L	L	H	Store Comparand to matched location, for purpose of setting Hit bit to "hit" value	4

Repeat above for each address filtering cycle

Notes:

1. Data on bus is unknown node address to be filtered or compared by CAM.
2. /EC pin brought LOW to enable Match flag during third cycle.
3. Some applications may only detect a match via the hardware match pin, /MF, and not need to read the software status match flag. If there is a match, this cycle isn't needed. If there isn't a match, then the MOV HM, CR will be ignored.
4. Sets Hit bit in Associated data field in the station list data word in LANCAM memory from the Comparand. The logic of this function is described in Section 3 of this Application Note.

Figure 4: Typical Address Filtering Code Sequence with "Node Address Learn Function"

Assumptions: This routine is similar to Figure 3 with the added function of "learning" or storing a non-matched Source address. The only change is to the last instruction which implements the store function in one cycle. The issue of this instruction by the local processor can be triggered by the "no match" indication in the Status register or the Match flag pin, /MF, remaining in the false state during the third data write cycle. See the MUSIC MU9C1480 LANCAM Handbook for timing details of /MF.

Cycle Type	Opcode or Data on Data Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Data Write	xxxxH	L	H	L	H	Input from local bus, generated from LAN bridge input, to Segment 1	1
Data Write	xxxxH	L	H	L	H	Input from local bus, to Segment 2	
Data Write	xxxxH	L	H	L	L	Input from local bus, to Segment 3	2
Command Read	Status	L	L	H	H	Output to data bus from Status register	3
Command Write	MOV NF, CR	L	L	L	H	Store Comparand to next free address	4

Repeat above for each address filtering cycle

Notes:

1. Data on bus is unknown node address to be filtered or compared by CAM.
2. /EC pin brought LOW to enable Match flag during third cycle.
3. Some applications may only detect a match via the hardware match pin, /MF, and not need to read the software match flag. A NOP taking /EC HIGH should be substituted for the Status Read in this case.
4. The source address in the Comparand register can be directly stored in the next free address in the array by this instruction, thereby "learning" the source address. If aging is implemented via a Hit bit which has been stored in the Comparand register's first segment, the source address entry is also automatically tagged "hit" by virtue of this store operation. The Full flag should also be tested at the same time as the Match flag to determine if a free address exists prior to attempting storage.

Figure 5: Example System Initialization Routine

Assumptions: Certain MUSIC MU9C1480 LANCAM memory locations are to be tagged as "RAM-only" for use as scratchpad memory locations for masks, etc. If no locations are to be so tagged, the instruction sequence defining and loading them can be omitted.

LANCAM locations to be used as "RAM-only" scratchpad are labeled xxx0H, xxx1H, xxx2H, xxx3H, etc. The local processor software logic will determine the total address values most convenient for the application.

Scratchpad location assignments:

0000H = Data for Hit = 0, used in Comparand Segment 0 to set Hit bit after address filter match
0001H = Data for Hit = 1, used in Comparand Segment 0 to set Hit bit after address filter match
0002H = Mask in MR1 to isolate Hit bit

This example also assumes that a vertically cascaded array is to be implemented; code is included to set the Page Address registers of each LANCAM.

Cycle Type	Opcode or Data on Data Bus	Control Bus /E	/CM	/W	/EC	Comments	Notes
Command Write	0000H	L	L	L	H	Allows for voltage memories and power up	
Command Write	TCO DS	L	L	L	H	Target Device Select register to disable local device select	
Command Write	FFFFH	L	L	L	H	Disable value	
Command Write	TCO CT	L	L	L	H	Target Control register for LANCAM Reset	1
Command Write	0000H	L	L	L	H	Control register value immediate field, reset value	1
Command Write	TCO PA	L	L	L	H	Target Page Address register to set LANCAM page for cascaded operation (if used)	2
Command Write	xxxxH	L	L	L	H	Page Address immediate field (if used) see the MU9C1480 LANCAM Handbook for detail	2
Command Write	SFF	L	L	L	H	Set Full flag to force operations to next LANCAM in array (repeat above 2 instructions for each successive device in array)	2
Command Write	TCO CT	L	L	L	H	Target Control register for LANCAM reset, to reset Full flags, Page Address, Device Select registers not affected	1
Command Write	0000H	L	L	L	H	Control register value immediate field, reset value	1
Command Write	TCO CT	L	L	L	H	Target Control register for all initial system values	3
Command Write	8040H	L	L	L	H	Control register value immediate field, see Handbook for bit assignments	3
Command Write	TCO SC	L	L	L	H	Target Destination Segment counter to set four segments for 64-bit memory writes	4
Command Write	18C0H	L	L	L	H	SC register immediate field, see the Handbook for bit assignments	4,6
Command Write	TCO AR	L	L	L	H	Target AR for initial address of scratchpad area	4
Command Write	0000H	L	L	L	H	Immediate field, initial address of RAM-only section	4
Command Write	SPD M@[AR],R	L	L	L	H	Set load memory relative to AR, set validity bits to RAM-only	4
Data Write	xxxxH	L	H	L	H	Load first mask or data value segment	4
Data Write	xxxxH	L	H	L	H	Second	4
Data Write	xxxxH	L	H	L	H	Third	4
Data Write	xxxxH	L	H	L	H	Fourth	4
Data Write	xxxxH	L	H	L	H	Load 1st segment of #2 mask or data	4
Data Write	xxxxH	L	H	L	H	2nd	4
Data Write	xxxxH	L	H	L	H	3rd	4
Data Write	xxxxH	L	H	L	H	4th	4
Data Write	xxxxH	L	H	L	H	Load 1st segment of #3 mask or data	4
Data Write	xxxxH	L	H	L	H	2nd	4
Data Write	xxxxH	L	H	L	H	3rd	4
Data Write	xxxxH	L	H	L	H	4th, etc.	4
		Continue loading as many locations as required by application					4
Command Write	TCO SC	L	L	L	H	Target Destination Segment counter start = 01, end = 11 for 48-bit Comparand writes, Source counter to start = 00, end = 00.	6
Command Write	3808H	L	L	L	H	Segment counter immediate field (see Handbook)	
Command Write	SPD CR	L	L	L	H	Set Comparand register as destination	
Command Write	MOV CR, aaaH	L	L	L	H	Target Comparand for move from scratchpad location containing proper Hit bit polarity in Segment 0	5
Command Write	0001H	L	L	L	H	Address of scratchpad location with Comparand Hit bit value	5
Command Write	SPS M@HM	L	L	L	H	Set Persistent Source to enable reading of 16-bit Associated data	

Figure 5: Example System Initialization Routine (Cont'd)

Notes:

1. The TCO CT immediate field bit assignments translate to 0000H for the reset condition. The default power-up condition generates the same effect, but good programming practice dictates a software reset to account for all possible conditions.
2. These cycles may be omitted for a single MU9C1480 application, since PA=0000H after a RESET.
3. Typical LANCAM control requirements could be:

Enable match flag	Enable address increment
Enable full flag	48 CAM bits, 16 RAM bits
Input not scrambled	Disable comparison masking (can be changed as required)

   See the MUSIC MU9C1480 LANCAM Handbook for bit assignments; this example translates to 8043H.
4. These cycles may be omitted if LANCAM Memory locations are not to be tagged as RAM-only for scratchpad usage. Conversely, if more are to be used and tagged, continue loading data values until selected number of locations are tagged and filled. Note that the instruction both accesses and tags as "RAM-only" in one operation.
5. Sends Hit bit in Associated data field to Comparand from the scratchpad location containing the proper polarity, enabling efficient tagging when compare is true. Location 0001H contains data value with "Hit" = 1. The logic of this function is described in Section 3 of this note.
6. The Segment Control register bit assignments for the first instance translate to 1800H and for the second instance translate to 3808H for this example; see the MUSIC MU9C1480 LANCAM Handbook for detail.

General:

Note that the MUSIC LANCAM need not have an SPD CR (Set Persistent Destination, Comparand) instruction presented to it as a command each time a compare is required. The SPD CR is required only to restore the Comparand register as the persistent destination if a previous Set Persistent Destination instruction was performed to force data to another destination in the LANCAM. A CMP (Compare) instruction is necessary only to force a comparison. Whenever the Comparand is the destination (as is the default case), a compare occurs automatically when the Segment Counter end count is reached, after which the Status register bits are appropriately set, and the /MF pin is asserted if enabled by taking /EC low on the last Data Write.

MUSIC Semiconductors®

USA Headquarters
MUSIC Semiconductors
254 B Mountain Avenue
Hackettstown, New Jersey 07840
USA
Tel: 908/ 979-1010
Fax: 908/ 979-1035

Asian Headquarters
MUSIC Semiconductors
Special Export Processing Zone
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 92 549 1480
Fax: +63 92 549 1024
Sales Tel/Fax: +632 723 62 15

European Headquarters
MUSIC Semiconductors
Torenstraat 28
6471 JX Eygelshoven
The Netherlands
Tel: +31 45 5462177
Fax: +31 45 5463663

MUSIC Semiconductors' agent or distributor:

http://www.music.com