Conversion of MU9C1480 LANCAM® to MU9C1480A/L LANCAMs®

Introduction

This Application Brief describes the ease with which a design may be moved from the MUSIC MU9C1480 LANCAM to the MUSIC MU9C1480A LANCAM. The enhanced features have been added in such a way that they do not affect the operation of nearly all existing applications.

The enhanced features are also available on the MU9C1480L, which may be used as a direct replacement when changing the system Vcc supply to 3.3 volts.

Pin Compatibility

The MU9C1480A and MU9C1480L LANCAMs are pin compatible with the MU9C1480 LANCAM provided that pins 35 (/RESET), 39 (/MA), and 40 (/MM) are left unconnected on the circuit board. The devices are designed in such a way that these signals can be left unconnected with no adverse effects on the CAM operation.

Software (Routine) Compatibility

The MU9C1480A and MU9C1480L LANCAMs have a superset of the MU9C1480 Instruction set; no instructions have been deleted, only added.

All existing MU9C1480 routines will run on the MU9C1480A/L devices.

The only caveats to the above statement are:

1. Command Reads from the Persistent Source register, where the device ID of 141H is found on bits 15–4.
2. Command Reads from the Status register, where the Validity Bits are found on bits 29–28.
3. Command Reads of the Next Free Address register, where the Page address is found on bits 15–11 when retrieving the Next Free address.

These locations previously returned values of 0 (zero). Command Reads of the first two cases are typically only found in qualification and diagnostic routines, and therefore should not affect the actual application. The third case may be an issue if the system needs to know the Next Free address and looks at bits 15–11 when retrieving the Next Free address.

One CAM/RAM partition configuration has been eliminated: 0 CAM, 64 RAM. This configuration was replaced with more useful RAM/CAM configuration options.

MU9C1480A/L Enhancements

➢ Dual Configuration Register Set

The Control, Segment Control, Mask Register 1, Address register, Persistent Source register, and Persistent Destination register are duplicated in the background register set to provide rapid context switching between the foreground configuration and the background configuration.

➢ Shiftable Comparand and Mask Register 2

The ability to shift the Comparand register and Mask Register 2 is useful in proximate matching algorithms.

➢ Increased CAM/RAM Partition Flexibility

There are now seven possible CAM/RAM configurations. Previously there were five possible configurations.

➢ /MA (Internal Match) and /MM (Internal Multi Match) Flag Outputs

Previously, the /MA and /MM flags were available through a Command Read of the Status register only. For some systems, the availability of these flags as hardware outputs improves system performance by reducing the number of Command Reads the processor needs to make when searching daisy-chained CAMs.

➢ MU9C1480A 70ns (Compare Cycle) Speed Grade

Previously, the fastest speed grade available was 90ns. The faster speed grade enables faster system speeds.

➢ Readable Device ID

A Command Read of the Persistent Source register will output the device ID of 141H on bits 15–4.

➢ Selectable Faster Operating Mode

Eliminates the need for a NOP after a no-match, improving routine execution time.

➢ Validity Bits Stored in Status Register

The Validity Bits of a memory location are stored in the Status register after a data read from memory, or move from memory operation.

➢ Single Cycle Reset of Segment Control Register

This single cycle reset of the segment counters in the Segment Control register reduces routine execution time in the case of interruptible routines.

➢ External Reset Pin

This reset works in parallel to the internal Power-On-Reset circuitry.

➢ Read of Next Free Address Register From Locked Daisy Chain

This allows the system to know the true Next Free address, including Page address, in case of daisy-chained CAMs with one Command Read. Previously, each CAM in the chain had to be polled individually.

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