What Is A CAM (Content-Addressable Memory)?

A CAM (content-addressable memory) is a memory device that accelerates any application requiring fast searches of a database, list, or pattern, such as in database machines, image or voice recognition, or computer and communication networks. CAMs supply the performance advantage over other memory search algorithms, such as binary or tree-based searches or look-aside tag buffers, by comparing the desired information against the entire list of pre-stored entries simultaneously, giving an order-of-magnitude reduction in the search time. CAMs are an outgrowth of RAM technology, thus to understand a CAM, it helps to contrast it with a RAM.

A RAM is an integrated circuit that stores data temporarily. Actually, RAM stands for random access memory, which emphasizes the ability to examine each stored piece of data independently of any other piece of data. Data is stored in a RAM at a particular location, called an address. So, in a RAM, the user supplies the address, and gets back the data. The depth of the memory, or number of locations, is limited by the ability to address the memory. For example, if the address bus (a bus is a group of signal lines entering or leaving a chip, or connecting a number of chips on a circuit board) is 8 bits wide, only 256 memory locations can be addressed, since in binary math, $2^8 = 256$. Binary math is used because signal lines normally have only two levels or states, HIGH and LOW. Thus if every line is moved from LOW to HIGH independently of every other line, 256 unique variations of the bus signal levels would exist, and each of those 256 variations would select one of the 256 memory locations. Address buses can be more than 8 bits wide. For example, 10 bits of address will allow you to select one of 1024 different locations; 16 bits selects one of 65,536 different locations; 20 bits selects one of 1,048,576 locations; and 32 bits selects one of over four billion locations. Each location is a place to store data: 1 bit per address, 4 bits per address (called a “nibble”), a byte (8 bits, or 2 nibbles) per address, a word (usually 16 bits) per address, or as wide as the data input bus allows. Common RAM chips today are organized as 262,144 locations (commonly called 256K) by 4 bits wide, or 1,048,576 locations (commonly called 1 Meg) by 1 bit wide, but other organizations are used in various applications, and larger sizes are announced on a regular basis. The depth of a memory system using RAM is limited by the number of address lines, but the width of the memory can be extended as far as desired.

RAM chips are composed of arrays of cells of transistors, each cell representing 1 bit, and containing one or more transistors depending on what kind of RAM it is: SRAM (Static RAM) or DRAM (Dynamic RAM). CMOS Static RAMs commonly use six transistors per cell, as shown in Figure 1; four are cross-coupled to store the state of the bit, and two are used to alter or read out the state of the bit. This configuration is called Static because the state of the bit remains at one level or the other until deliberately changed, or power is removed. Dynamic RAMs, on the other hand, are named for the transient nature of their storage mechanism, which commonly consists of a single transistor along with a capacitor to store the bit information. During a read, the charge on the capacitor is drained to the bit line, requiring a rewrite of the bit, called a restore operation. Additionally, because the DRAM capacitor is not perfect, it loses charge over time and needs to have its charge refreshed at regular intervals. Thus, dynamic memories are accompanied by controller circuits to rewrite the bit and refresh the stored charge on a regular basis. In spite of the added complexity of the memory control, the simplicity of the DRAM cell itself explains the higher density and lower cost of DRAMs versus SRAMs. Neither SRAMs nor DRAMs retain information when power is removed; but with battery backup, SRAMs are often used to store important configuration information when main power is removed because they do not require refreshing.

Content-addressable memories (CAMs) are organized differently. In a CAM, data is stored in locations in a somewhat random fashion. The locations can be selected by an address bus, or the data can be written directly into the first empty location, because every location has a pair of special status bits that keep track of whether the location has valid information in it or is empty and available for overwriting. Once information is stored in a memory location, it is found by comparing every bit in memory with data placed in a special Comparand register. If there is a match for every bit in a location with every corresponding bit in the Comparand, a Match flag is asserted to let the user know that the data in the Comparand was found in memory. A priority encoder sorts out which matching location has the top priority, if there is more than one, and makes the address of the matching location available to the user. Thus, with a CAM, the user supplies the data and gets back the address. Because the CAM does not need address lines to find data, the depth of a memory system

using CAMs can be extended as far as desired, but the width is limited by the size of the chip. For example, the MUSIC MU9C1480A LANCAM is 64 bits wide, but 1024 entries deep. To extend the depth is a simple matter, because the addressing is all self-contained. To extend the width takes additional routines due to the difficulty in extending 1024 match lines from chip to chip.

CAMs are based on memory cells that have been modified by the addition of extra transistors that compare the state of the bit stored with the state stored in a Comparand register. Logically, CAMs perform an exclusive-NOR function, so that a match is only indicated if both the stored bit and the corresponding Comparand bit are the same state. The MUSIC MU9C1480A LANCAM uses ten-transistor cells similar to that shown in Figure 2, composed of a six-transistor SRAM memory cell plus four transistors to accomplish the exclusive-NOR function and match line driving, which results in what is called a Static CAM cell. For writing and reading, each Static CAM cell acts like a normal SRAM cell, with differential bit lines to latch the value into the cell when writing, and sense amps to detect the stored value when reading. When writing, the word line is energized, turning on the pass transistors that then force the cross-coupled transistors to the levels on the bit lines. When the word line is de-energized, the cro ss-coupled transistors remain in the same states. For reading, the bit lines are pre-charged to the same intermediate voltage level, the word line is energized, and the bit lines are forced to the levels stored by the cross-coupled transistors. The sense amps respond to the difference in the bit lines and report the stored state to the outside world. For comparing, the match line is pre-charged to a high level, the bit lines are driven by the levels of the bit stored in the Comparand register, but the word line is not energized, so the state of the cross- coupled transistors is not affected. The exclusive-NOR transistors compare the internally stored state of the cross-coupled transistors with the levels of the Comparand bit, and if they do not agree, the Match line is pulled down, indicating a non-matching bit. All the bits in a stored entry are connected to the same Match line, so that if any bit in a word does not match with its corresponding Comparand bit, that Match line is pulled down. Only the entries where the Match line stays HIGH are considered matches. All the Match lines are fed to a Priority encoder that determines whether any match exists, whether more than one match exists, and which matching location is considered the highest priority.

A DCAM, or Dynamic CAM, cell is also possible, which a user might expect to be simpler than a Static CAM cell, but having the refresh requirements similar to a DRAM cell. Various proposed designs have been put forth, such as the Mundy or Wade-Sodini cells described in the paper by John Wade and Chuck Sodini [1]. MUSIC holds a DCAM cell patent for a five-transistor cell [2]. One advantage that a DCAM cell has over a Static CAM cell is the ability to store "don't cares." Since the DCAM only looks at the difference in charge stored on two capacitors, both capacitors can have the same charge or different charge. A difference can indicate a 1 or a 0, depending on the direction of the difference. But when they are the same charge, two additional states are available which are neither a 1 nor a 0, and one is selected to be a "don't care." For an NMOS XNOR gate, both capacitors must store a 0 for a "don't care." The same function can be performed by two Static CAM cells to give four states, as described in the paper by Sergio Ramirez-Chavez [3].

Refer to Teuvo Kohonen's "Content-Addressable Memories" (Second edition, Springer-Verlag, 1987) for additional source material on CAM technology.

[1] J. Wade and C. Sodini, "Dynamic cross-coupled bit-line content addressable memory cell for high-density arrays," IEEE Journal of Solid State Circuits, Vol. SC-22, February 1987.

[2] U.S. Patent #4791606

[3] Sergio R. Ramirez-Chavez, "Encoding 'Don't Cares' in Static and Dynamic Content-Addressable Memories," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 39, No. 8, August 1992.

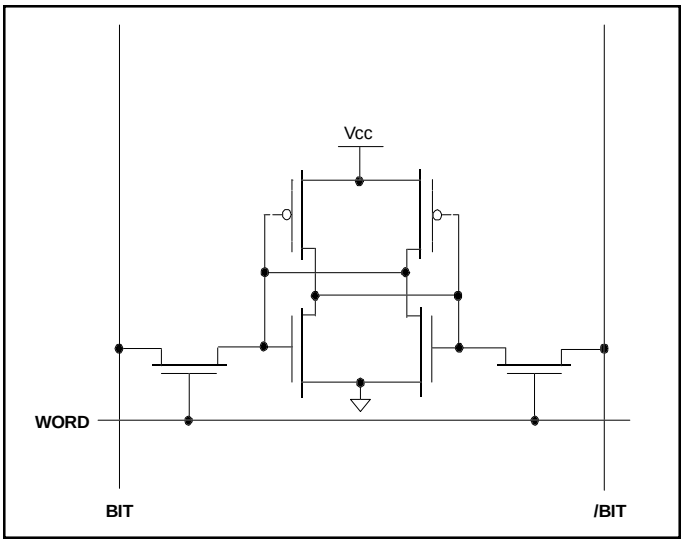

Figure 1: Typical CMOS SRAM Memory Cell

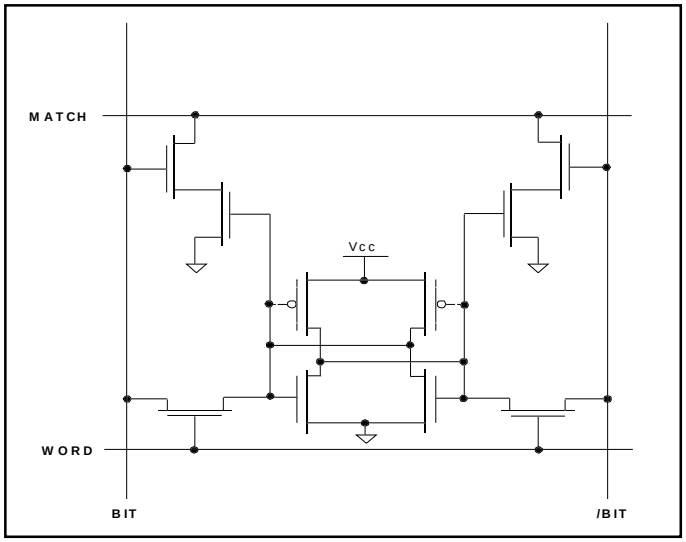

Figure 2: Typical CMOS Static CAM Memory Cell

NOTES

MUSIC Semiconductors Agent or Distributor:

MUSIC SEMICONDUCTORS

http://www.music-ic.com
email: info@music-ic.com

USA Headquarters
MUSIC Semiconductors
254 B Mountain Avenue
Hackettstown, New Jersey 07840
USA
Tel: 908/979-1010
Fax: 908/979-1035
USA Only: 800/933-1550 Tech. Support
888/226-6874 Product Info.

Asian Headquarters
MUSIC Semiconductors
Special Export Processing Zone 1
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 49 549 1480
Fax: +63 49 549 1023
Sales Tel/Fax: +632 723 62 15

European Headquarters
MUSIC Semiconductors
Torenstraat 28
6471 JX Eygelshoven
Netherlands
Tel: +31 45 5462177
Fax: +31 45 5463663