Reading Out The Valid LANCAM® Memory Entries

The MU9C1480A LANCAM is a versatile content-addressable memory that features automatic comparisons and a powerful Write at Next Free Address instruction, which makes it ideal for keeping address lists in LAN switch and router applications. Because it holds 1024 entries, housekeeping routines are necessary to keep things manageable such as applying aging algorithms. Such algorithms will keep only recently used entries VALID in memory, while aged entries are invalidated, or declared empty. On occasion, the Network Manager may wish to retrieve a list of the currently Valid addresses stored in the station list in a vertically cascaded string of LANCAMs to store in a backup list, or for other monitoring purposes. Since many switch and router applications have large station lists, doing a DMA-type dump of all entries of the CAM memories (which is certainly feasible with the built-in Address counter of the LANCAM) without regard to whether they are current or not, would be tedious. But the versatile LANCAM has commands built into it to simplify reading out only the Valid entries.

The routines shown in Routines 1 through 4 on page 3 assume a vertically cascaded string of LANCAMs that have been configured for 48 bits of address filtering, with automatic readout of the 16-bit Associated Data field. Each device has been assigned a Page Address value starting with 0000H. As the network address data is entered into the Comparand register, an automatic comparison occurs with the entire contents of the string on the last segment load, a match indicated by the /MF flag, and the Associated data read from the Highest-Priority Match address. Nonmatching addresses are learned by the use of the MOV NF, CR, V instruction. This process continues until some housekeeping is required or on a regular basis, usually 300 seconds.

Now, let's interrupt this process to read out the list of VALID entries. Looking at the procedure in Routine 1, you can see that we need to change some of the register values to allow us to read out the 48 bits of address information stored in all the Valid entries in the string. The first command (TCO DS, FFFFH) selects all devices in the string. The next command (TCO CT, FFDFH) tells the Control registers to do all comparisons through Mask Register 1. Lines 5 and 6 show the TCO SC, 39C9H command that sets the Segment Control register for three segment writes (Destination) and three segment reads (Source). And finally, the SPD MR1 command is used with the next three Data Writes to load Mask Register 1 with an opaque mask of all 1s, which will force the data portion of all entries to match, since only the Validity bits are of interest, not the contents. Finally, the Persistent Destination for Data Writes is returned to the Comparand register with a SPD CR instruction to prepare for the return to normal operation.

Routine 2 shows a procedure to find and output all the Valid entries, device by device, by examining the Status register after every compare to see if a match has occurred. The Status register will also tell you by indicating a no-match condition that you have looked at every Valid entry in that particular device and to select another device. This procedure is useful if you want to use the Data bus to read out match conditions, rather than utilize the hardware-based daisy chain feature of the LANCAM involving /EC and /MF, as shown in Routine 3.

In the approach shown in Routine 2, we start out by selecting the first device in the string with a TCO DS, 0000H command. Next we perform a comparison on the validity bits (CMP V), which compares all Valid entries against the Comparand register through the opaque mask. The Highest-Priority Valid entry address is loaded into the Status register, which is examined, not for that address, but for bit 0, which tells us if a match actually occurred. If that bit is not LOW, then no match was found, and no Valid entries exist in that device. If there was a match indicated by a LOW in bit 0, three data reads are performed to get the 48-bit address entry onto the data bus, starting with Segment 1 (lowest order) and automatically incrementing to Segments 2 and 3 (highest order). Then, to find the next Valid entry, we set this entry to skip with a VBC HM,S command. (We will reset it to valid later.) Now, we repeat the exercise starting with the CMP V command again. This time, the entry we found last time is skipped over, and the next Valid entry becomes the Highest-Priority match. To select the next device in the string because all the matching entries have been found in the first device, go back to the top of this procedure and select the next device with a TCO DS, 0001H and repeat the matching procedure until all the Valid entries in device 0001H have been found, and so on until all the devices in the string have been examined. Then the skipped entries are returned to Valid utilizing the procedure shown in Routine 4. If at any time during this matching procedure, we need to abort the routine and go back to normal bridge-type operation, we jump immediately to the procedure in Routine 4, and execute its command sequence to get back into a normal mode of operating.

The procedure in Routine 3 accomplishes the same thing as the procedure in Routine 2, but uses the daisy chaining capability of the LANCAM. This procedure is faster because it eliminates selecting each device individually and reading the status registers to determine whether a match occurred. The Valid entries in the entire string are found automatically using the /EC control signal and monitoring the hardware daisy chain output signal /MF. Because all devices in the string are still selected from the procedure in Routine 1, a CMP V executes on all devices simultaneously. Taking /EC LOW locks the /MI–/MF daisy chain in this procedure, so that only the device with its /MI HIGH and its /MF LOW will respond to the following Data read. The /MF pin of the final device in the chain gives the system Match flag for the entire daisy chain, and as long as there is a match anywhere in the chain and /EC is LOW, the final /MF will be LOW. The first match will likely be the device at the top of the string, since /MI is normally tied HIGH for that device. The next three Data reads will give back the 48-bit address stored in the Highest-Priority Valid entry in that device, starting with Segment 1 (lowest order) and automatically incrementing to Segment 3 (highest order). /EC is kept LOW to keep the daisy chain locked onto this device. After reading the entry, it is set to skip with a VBC HM,S command. (We will reset it to Valid later.) The exercise is repeated starting with the CMP V command, keeping /EC LOW. Only the device that responded previously will execute the CMP V this time, but if all the Valid entries in this device have been found, no match will occur, so the next device in the chain with a Valid entry will respond to the Data reads. This procedure is repeated until the /MF line goes HIGH, indicating all the Valid entries in the entire string of LANCAMs have been found. The string is returned to normal operation by jumping to the CMP S instruction in Routine 4. If at any time during this procedure, we need to abort the routine and go back to normal bridge-type operation, a jump to line 28 is used in the procedure in Routine 4, to get back to a normal mode of operating.

The procedure in Routine 4 returns the string of devices to normal operation, with 48-bit writing to the Comparand. The procedure in Routine 4 returns the string of devices to normal operation, with 48-bit writing to the Comparand register and 16-bit reading of the associated data of the highest-priority match, with no masking. The first command (TCO DS, FFFFH) selects all the devices. This is needed for a return from the procedure of Routine 2, but not from the procedure of Routine 3. The second command, CMP S, finds all the entries in all the devices that have been set to skip. The next command (VBC ALM,V) then resets all the skipped entries to Valid in all the devices. The next two commands reset the Control register and the Segment Control registers to their original settings for normal operation.

Note: These examples use the LANCAM Standard mode. The Enhanced mode of the A/L LANCAM could be used to somewhat supply these routines. Please consult with MUSIC Semiconductors' Technical Support for any questions.

Line	Cycle	Command	/EC	Comments
1	CW	TCO DS	H	Targets Dev. Sel. reg.
2	CW	FFFFH	H	Selects all devices
3	CW	TCO CT	H	Target Control reg.
4	CW	FFDFH	H	Sets MR1 for Compares
5	CW	TCO SC	H	Targets Seg. Cont. reg.
6	CW	39C9H	H	3 Seg. Writes and Reads
7	CW	SPD MR1	H	Selects MR1 for DWs
8	DW	FFFFH	H	Loads Opaque mask into
9	DW	FFFH	H	upper 48 bits
10	DW	FFFFH	H	
11	CW	SPD CR	H	Sets Destination for Data Writes to Comp. reg.

Routine 1: Set Up All Devices to Read Out Stored Entries

Line	Cycle	Command	/EC	Comments
12	CW	TCO DS	H	Targets Dev. Sel. reg.
13	CW	0000H	H	PA of first device
14	CW	CMP V	H	Finds first Valid entry
15	CR	ssss	H	Read Status reg. for match
16	DR	dddd	H	Read Seg 1
17	DR	dddd	H	Read Seg 2
18	DR	dddd	H	Reg Seg 3
19	CW	VBC HM,S	H	Set this entry to Skip
•	•	•	•	Repeat lines 14–19 until
•	•	•	•	no match is found

Repeat this procedure starting at line 12 for each device in the string by incrementing the Device Select value in line 13 above. When done, or to abort, jump to line 26.

Routine 2: Procedure to Find Valid Entries Using the Status Register

Line	Cycle	Command	/EC	Comments
20	CW	CMP V	L	Find first Valid entry
21	DR	dddd	L	Reads Seg 1
22	DR	dddd	L	Reads Seg 2
23	DR	dddd	L	Reads Seg 3
24	CW	VBC HM,S	L	Set this entry to “Skip”
•	•	•	•	Repeat lines 20–24 until
•	•	•	•	/MF stays high
25	CW	NOP	H	Unlocks daisy chain

Jump to line 28 to return to normal operation, or to abort.

Routine 3: Procedure to Find Valid Entries Using the Daisy Chain

Line	Cycle	Command	/EC	Comments
26	CW	TCO DS	H	Targets Dev. Sel. reg.
27	CW	FFFFH	H	Selects all devices
28	CW	CMP S	H	Finds Skipped entries
29	CW	VBC ALM,V	H	Resets all Skips to Valid
30	CW	TCO SC	H	Targets Seg. Cont. reg.
31	CW	3808H	H	3 Seg. Write/1 Seg. Read
32	CW	TCO CT	H	Targets Control reg.
33	CW	FFCFH	H	Resumes No Masking

Routine 4: Return the String of Devices to Normal Operation

NOTES

MUSIC Semiconductors Agent or Distributor:

MUSIC SEMICONDUCTORS

http://www.music-ic.com
email: info@music-ic.com

USA Headquarters
MUSIC Semiconductors
254 B Mountain Avenue
Hackettstown, New Jersey 07840
USA
Tel: 908/979-1010
Fax: 908/979-1035
USA Only: 800/933-1550 Tech. Support
888/226-6874 Product Info.

Asian Headquarters
MUSIC Semiconductors
Special Export Processing Zone 1
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 49 549 1480
Fax: +63 49 549 1023
Sales Tel/Fax: +632 723 62 15

European Headquarters
MUSIC Semiconductors
Torenstraat 28
6471 JX Eygelshoven
Netherlands
Tel: +31 45 5462177
Fax: +31 45 5463663