

Application Brief AB-N12

USING THE MU9C1965A/L LANCAM® MP IN LAN-ATM EDGE SWITCHES

INTRODUCTION

This Application Brief covers the use of the MU9C1965A/L content-addressable memory (CAM) in ATM edge switches. The width of this device, 128 bits, makes it possible to use it for translating from 48-bit LAN source and destination addresses to ATM cell headers. Since ATM headers identify the connection, rather than either the source or destination alone, a single 48-bit address does not suffice; both the source and destination must be used. The unique ability of MUSIC CAMs to supply data from the remainder of the 128-bit width is a great benefit here: on the next cycle, 32 bits of data are available from the CAM without further table lookups. Hence the ATM virtual path and virtual connection information are available immediately. In the reverse direction, the cell header is used as input to the CAM and 96 bits of LAN source and destination are retrieved. This facility is valuable both in edge switches operating with wide-area ATM networks and in LAN emulation, in which both ATM and conventional LAN devices are supported in the same network.

BENEFITS OF CAM

Unlike any other form of computer memory, CAM does not only consist of a set of storage locations accessed by an address. Instead, it is addressed by its contents, hence the name content-addressable memory, or CAM.

The data to be processed is stored in a special register, the Comparand; during one single cycle the incoming data is compared with all the valid entries stored within the CAM. This is extremely fast, since the comparison operation is done completely in hardware at the gate level and all locations are compared simultaneously with the comparand. A flag is set for each location that matches the comparand, and the locations of the flags are then read out. Because the operation is carried out in parallel for all locations on the chip, the results are available in a few tens of nanoseconds, regardless of the length the entire list is. In addition, there is never any overhead required to sort the data in the CAM; access is equally fast no matter in what order the data resides in the CAM chip. The search speed is thousands of times faster than sequentially searching a set of database records, and a great deal faster than microcode-based searching in a device controller.

CAMs are particularly useful in networking applications because of the extensive use of various types of addresses. These addresses have been adopted by different groups of implementers or standards drafters at different times for different purposes, resulting in many incompatible formats. Yet it is necessary to interoperate with several types of addressees in most applications. Since addresses can be very readily accessed in a CAM, the complex job of manipulating addresses is considerably simplified.

In addition to its speed, a CAM provides a very compact implementation that minimizes board real estate for the search operation. Compared to conventional static RAM searched by a microprocessor, CAM offers both speed and a much smaller footprint on the board, perhaps only a single chip. Design and layout are correspondingly easier to do, and the associated software or firmware is much simpler.

There are other ways to get the same job done. Linear lists and binary trees are options, but not practical for networking needs. The only alternative to the CAM is the use of hash tables. As each data item is stored, its storage location is determined by some function of the key. If the data space is sparsely populated (the general case for networking applications), hash coding provides an easy way to compact the storage space.

But if the address is shortened, then there is a risk that two or more data items will hash to the same location. The solution to this problem is to store the key and its associated data in the next free location in memory, should the first location already be occupied. Then when searches are done, the comparand will hash to the first location; if the key stored there proves to be the wrong one, then a linear search is undertaken until the right key is retrieved. Needless to say, this approach suffers severe limitations, in terms of speed and flexibility. In addition, hashing techniques do not offer masking capabilities, and addresses of different nature can not be held in the same list.

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MUSIC'S UNIQUE FEATURES

128-Bit Width

The MUSIC MU9C1965A/L LANCAM MP is a CAM designed for the special needs of state of the art data networking. It is unique in its width of 128 bits, the widest in the industry. This allows a great deal of flexibility in terms of what types of addresses and other information can be used to form the search key. Frequently this will make it possible to access in one step information that otherwise would take two or three search steps; this translates into a significant saving in time and in the hardware needed for the search steps.

Direct Access to Data

In addition, MUSIC has a patented capability of flexibly partitioning the CAM into two regions: the comparand and data that is not part of the search. Should the full 128-bit width of the 1965A/L not be needed for the search keys, the width of the chip can be divided into CAM and RAM, under program control. For example, if the desired key width is 96 bits, then the remaining 32 bits of each location can be used to store associated data. Rather than using a second table lookup to get the data from static RAM with parallel addresses, the data can be obtained directly from the CAM. Once again, significant amounts of time and hardware are saved.

Also, masks are available to limit the search to a subset of bit positions, if desired. This enables the designer to set up arbitrary bit positions as match-required and the remainder as "don't care" positions.

Shifting Capability

Another unique feature of the 1965A/L is the ability to try again, with the comparand shifted. In cases where several search patterns differ by a shift operation, the comparand can be shifted and tested again with minimum overhead between operations. This can be repeated as often as necessary. This feature is particularly useful in pattern matching applications, where the trial pattern may be offset from the master due to uncertainties in the start of the scan. With the shifting capability, the trial pattern slides sideways until a match occurs or no match is found at all.

APPLICATION: THE ATM EDGE SWITCH

A prime area of applicability for the 1965A/L is in an ATM edge switch. An edge switch sits at the edge of an ATM network, typically receiving data from users either over LANs or over point-to-point lines. This is shown in Figure 1.

An edge switch has a number of functions that are required at the periphery of an ATM network, but are not needed in the internal switches of the network. These include:

- Address translation from LAN to ATM formats
- User validation (particularly for public networks)
- Bandwidth Monitoring

In all of these operations, CAMs are useful in the edge switch. As a general rule of thumb, the greater the difference between two networking technologies, the more benefits a CAM provides.

In this case, the addressing of interest is the LAN address vs. the ATM header. In the LAN case, the address is a true address in the sense used by the Post Office: the same address is used to reach a person, regardless of who is sending mail. In the ATM case, however, the cell is too small to carry a full address in the header; instead it has a connection identifier in the header that is reassigned switch by switch. LANs are connectionless, fully addressed in each packet; ATM is connection-oriented, with the full address used only at connection setup time. Given the large difference in approach, it is not surprising that CAMs are very useful at the boundary between the LAN and ATM.

LAN-TO-ATM MAPPING

LAN Addresses

The MAC address used on LANs is 48 bits long, counting the bits for local/universal address and individual/group (multicast) address. These addresses are unique by nature–no two LAN interfaces should ever have the same one.

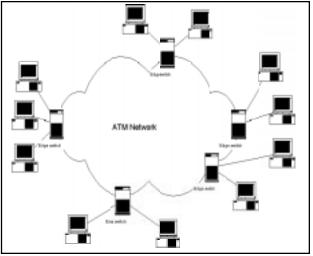


Figure 1: ATM Network

Figure 2 shows the Universal LAN address format, used by Ethernet, token ring, and other standard LANs. Note that this is not the transmission order; within each byte, the least-significant bit is sent first.

ATM Addresses

In the case of ATM networks, the ability to intermix a variety of traffic types is facilitated by sending data in small cells with 48 bytes of payload. This small size provides assurance that delay-critical applications like voice will not be impacted by long data packets that cannot be interrupted. A connection-oriented approach is used, in which the cell header is really a connection number having only a local meaning, from one switch to the next one.

Note: ATM does have an address in the normal sense: it is the 60-bit address specified in ITU Recommendation E.164. This address is unique for each end point, regardless of where the connection originates. E.164 addresses are mainly used for connection setup purposes.

Once the connection is set up (which can be on a permanent or switched basis like a dialed phone call), a connection identifier is used at each switch to route the cells. This field is divided into a Virtual Path Identifier (VPI) of 8 bits or 12 bits and a Virtual Channel Identifier (VCI) of 16 bits.

Figure 3 shows the Header formats for User-to-Network Interface (UNI) and Network-to-Network Interface (NNI).

| bits 1 | 1 | 22 | 24 |
|--------|-----|----------------|--------------------------|
| i/g | u/l | manufacturer # | assigned by manufacturer |

Figure 2: Universal LAN Address Format

| | bits 4 | 8 | 16 3 | | 1 | | 8 | | 424 (48 bytes) | | |
|---|-------------------|---|-------|---|----|-----|---|-----|----------------|----------------|--|
| | GFC | - | | - | _ | | - | _ | | DATA | |
| | UNI HEADER FORMAT | | | | | | | | | | |
| ſ | bits 12 | | 16 | 3 | ; | 1 | | 8 | | 424 (48 bytes) | |
| ľ | VPI | | VCI P | | ΓI | CLP | | HEC | | DATA | |
| L | NNI HEADER FORMAT | | | | | | | | | | |

Figure 3: Header Formats

The handling of calls can be on a Virtual Channel basis, in which all VPI/VCI bits are used in the switching process, or as a Virtual Path in which switching is done on the VPI field only and the customer could use the VCI field for private multiplexing. Since these fields are small, uniqueness in the LAN style is not possible. They are assigned by individual switches and in fact can be the same on different ports of the switch. As a cell goes through the network, its VPI and VCI values in general are remapped at each switch, a process usually referred to as VPI/VCI Translation.

Interworking Between LANs and ATM

There are several ways to provide interoperability between LANs and ATM. A typical way to interconnect the LAN and ATM portions of the network is to do address translation. On arriving at the ATM edge switch, the packet's LAN address is translated to an ATM VPI/VCI. At the far end of the ATM network, the reverse translation is done.

However, the VPI/VCI header is a connection identifier, not an address in the normal sense. If two stations are sending data to the same destination, they do not use the same cell header. These are two different connections and they must have different cell headers to enable the cells to be reassembled correctly. In other words, the cell header encodes both the source and destination.

This is in contrast to a typical LAN bridge or switch. Where as only the destination address needs to be looked at to direct the packet to the correct destination. The source address simply rides in the packet, to be used by the destination to route the packet to the correct file transfer application, or whatever. The connection based native of ATM requires that both SA and DA are used to identify a connection. As a result, a total of 96 bits must be used as the search key.

With a width of 128 bits, the 1965A/L is able to accommodate the 96-bit comparand formed from the combined LAN Source and Destination Addresses. In the remaining 32 bits, there is room for the associated VPI/VCI, together with other important information like the outgoing port number and priority index. This information is available in the same cycle, with no further table lookup needed. The mapping is shown schematically in Figure 4.

| 96 bits fo | 32 bits for data | | | |
|-----------------|-------------------|-----|-----|--------|
| DEST ADDRESS | SOURCE ADDRESS | VPI | VCI | Others |

Figure 4: CAM Contents For LAN To ATM Mapping

MAPPING ATM TO LAN ADDRESSES

At the far end of the ATM network, the reverse mapping must be made. The ATM cell header must be used as the key in order to retrieve the original LAN source and destination addresses.

If the need for associated data exceeds DA and SA, a 32-bit CAM such as the MUSIC MU9C4320L is used with the cell header as the comparand, and the unused bits masked out. A match from this CAM access provides an index into an SRAM containing the LAN addresses and any other associated data of any practical length.

If only SA and DA need to be retrieved, the 1965A/L can be used in what is essentially the inverse of the original mapping process. The CAM is set up for 32-bit comparands (again masked to the desired number of bits such as 24 or 28) and the remaining 96 bits used to contain the LAN source and destination addresses. Only one cycle (70 nanoseconds) is used for the whole process. This is the most compact and simple method of all.

CODING EXAMPLES

CAM Configuration

Foreground (SFR): DA, SA to VPI/VCI

data destination is CR, segments 0-3 data source is HM, segment 0 96 bits CAM, 32 bits RAM; no mask register

Background (SBR): VPI/VCI to DA, SA

data destination is CR, segment 0 data source is HM, segments 0–3 96 bits RAM, 32 bits CAM; use Mask Register 1

Routine 1: LAN to ATM

CWS (SFR)//Set Foreground configuration DWS (SEG 0)//dummy write DWS (SEG 1)//write 32 bits DA DWS (SEG 2)//write 16 bits DA, 16 bits SA DWLEC (SEG 3)//write 32 bits SA and Compare DRL (SEG0)//get port ID, VPI/VCI

Routine 2: ATM to LAN

CWS (SBR)//set Background configuration DWS (SEG 0)// write VPI/VCI and Compare DRL (SEG0)// get port ID DRL (SEG 1)//get 32 bits DA DRL (SEG 2)//get 26 bits DA, 16 bits SA DRL (SEG 3)//get 32 bits SA

Routine 3: Add Connection

CWS (SFR)//set Foreground configuration DWS (SEG 0)//write port ID and VPI/VCI DWS (SEG 1)//write 32 bits DA DWS (SEG 2)//write 16 bits DA, 16 bits SA DWS (SEG 3)//write 32 bits SA CWL (MOV_NF_CR_V)//move to the next free location

Routine 4: Delete Connection

CWS (SBR) //Set Background configuration CWS (SEG 0) // write VPI/VCI CWL (VBC_HM_E)

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|--|--|--|---|--|--|
| | USA Headquarters MUSIC Semiconductors | Asian Headquarters MUSIC Semiconductors | European Headquarters MUSIC Semiconductors | | |
| | 254 B Mountain Avenue | Special Export Processing Zone 1 | Torenstraat 28 | | |
| | Hackettstown, New Jersey 07840 | Carmelray Industrial Park | 6471 JX Eygelshoven | | |
| SEMICONDUCTORS | USA | Canlubang, Calamba, Laguna | Netherlands | | |
| | Tel: 908/979-1010 | Philippines | Tel: +31 45 5462177 | | |
| http://www.music-ic.com | Fax: 908/979-1035 | Tel: +63 49 549 1480 | Fax: +31 45 5463663 | | |
| email: info@music-ic.com | USA Only: 800/933-1550 Tech. Support | Fax: +63 49 549 1023 | | | |
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