MUSIC SEMICONDUCTORS

Application Brief AB-N1

The MUSIC LANCAM® Family

The MUSIC LANCAM® Family consists of devices specifically designed to accelerate the performance of LAN switches and routers. These MUSIC devices are optimized to various functions without excessive external hardware or software overhead, at the highest level of performance.

Functions	LANCAM Features
The ability to store any sizable station list.	Large CAM array, up to 8K x 64, targets the need of switches and rotuers to store any sizable station list. Simple vertical cascading in a daisy chain fashion extends CAM memory depth., without any external logic.
Implement transparent learning efficiently.	Facilitates transparent SA learning with a Store at Next Free Address instruction (fast, single cylce learn mode).
Store access history (aging) information about each node quickly to allow purging of aged entries to minimize memory (CAM) requirements.	Can tag or time stamp each entry as accessed (hit) during a match cycle with one additional cycle, due to CAM/RAM partitioning capability; no need for external mirror RAM.
Perform fast purging based on access history without memory contention with real-time network filtering.	All aged entries can be purged by aging algorithms in less than 1.5 microseconds due to a powerful and flexible instruction set. Ability to designate any CAM 64-bit locations as RAM-only for scratchpad use facilitates this fuction; allows 64-bit moves in one cycle; eliminates the need to load masks in real-time through a 16-bit bottleneck via the MOV instructions.
Store node or port attributes efficiently to facilitate multi-port switches and routers and be able to read attributes quickly to minimize memory contention and resulting network congestion.	Node attributes (port address, access history (aging), port protocol (FDDI, Token, Ethernet, etc.)) can be stored in the same location as the station address and read in one cycle via the associated data storage facility (persistant read of memory function and the CAM/RAM partition capability). Two segment counters allow read attribute after write and match of CAM data without extraneous setup cycles. Two mask registers facilitate many functions such as aging, node attribute read, group location, etc..
Handle multi-protocols (Ethernet and Token ring) efficiently.	Internal translation switch translates between Ethernet and Token Ring on the fly.
Perform all the previous functions fast enough to eliminate or minimize network congestion at any LAN wire speed.	Please refer to the LANCAM Selection Guide for performance information.

ADDITIONAL FEATURES OF THE LANCAM

- Supports bulk DMA loading or readback of lists via an auto-incrementing/auto-decrementing internal Address register.
- CAM/RAM partitioning capability and Status bits enable locations to be tagged to support any routing function. Status bit (Validity bit) control instructions and ability to explicitly compare on skipped, empty, or RAM-only locations facilitates this and other functions.
- Diagnostics are facilitated by the flexible instruction set and ability to perform internal 64-bit moves to/from key registers and compare explicitly.
- Context-specific functions are facilitated by the ability to read/write to a specific CAM in a cascaded array via a software accessible device address.

TYPICAL ADDRESS FILTERING CODE SEQUENCE WITH NODE ADDRESS LEARN FUNCTION

The following routine illustrates the address filtering input sequence with the additional functions of learning or storing a non-matched Source address. The issue of this instruction by the local processor can be triggered by the no match indication in the Status register or Match Flag pin, /MF, remaining in the false state during the third data Write cycle.

Cycle Type	Opcode or Data on Data Bus	Control Bus				Comments	Notes
		/EC	/CM	/W	/E		
Data Write	xxxxH	L	H	L	H	Input from local bus, generated from LAN port, segment 1	1
Data Write	xxxxH	L	H	L	H	Input from local bus, segment 2	
Data Write	xxxxH	L	H	L	L	Input from local bus, segment 3	2
Command Read	Status	L	L	H	H	Output to data bus from Status register	3
Command Write	MOV NF, CR	L	L	L	H	Store Comparand to Next Free address	3

Repeat above for each address filtering cycle.

Notes:

1. Data on bus is unknown node address to be filtered or compared by CAM.
2. /EC pin brought LOW to enable Match flag during third cycle.
3. If previous Status Read operation or the hardware Match flag, /MF, indicates a no match condition, the Source address in the Comparand register can be directly stored in the Next Free address in the array by this instruction, thereby learning the Source address. If aging is implemented via a Hit bit that has been stored in the Comparand register's segment 0, the source address entry is also automatically tagged "hit" by virtue of this store operation. The Full flag should also be tested at the same time as the Match flag to determine if a free address exists prior to attempting storage.

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