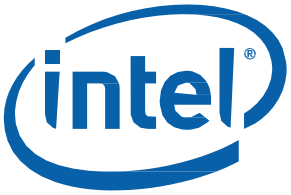

Intel® Ethernet Connection I218/I219 Specification Update

July 2017
Revision 1.3

Revision History

Date	Revision	Description
April 2013	1.0	Initial Release (Intel Public).
May 2015	1.1	Second Release (Intel Public).
June 2017	1.2	Third Release (Intel Public).
July 2017	1.3	Fourth Release (Intel Public).

Note: This page intentionally left blank.

1.1 Introduction and Scope

This document applies to the Intel® Ethernet Controller I218/I219.

This document is an update to a published specification, the *Intel® Ethernet Controller I218/I219 Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.2 Product Code and Device Identification

Product Codes: WGI218LM/ WGI219LM and WGI218V/WGI219V (Commercial Copper).

The following tables and component drawings describe the various identifying markings on each device package:

Table 1-1 Markings

Device	Stepping	Top Marking	Description
I218LM	B1	WGI218LM	Production Commercial Copper
I218V	B1	WGI218V	Production Commercial Copper
I219LM	A0	WGI219LM	Production Commercial Copper
I219V	A0	WGI219V	Production Commercial Copper

Table 1-2 Device IDs

I218/I219 Device ID Code	Vendor ID	Device ID
I218LM	0x8086	0x155A, 0x15A0, 0x15A2
I218V	0x8086	0x1559, 0x15A1, 0x15A3
I219LM	0x8086	0x156F, 0x15B7, 0x15D7, 0x15E3, 0x15B9
I219V	0x8086	0x1570, 0x15B8, 0x15D8, 0x15D6

Table 1-3 MM Numbers

Product	MM Number	Intel Spec Code	Media
WGI218LM (Production Commercial Copper)	926895	SLJK3A	Tape & Reel
WGI218LM (Production Commercial Copper)	926892	SLK3B	Tray
WGI218V (Production Commercial Copper)	926893	SLK3C	Tape & Reel
WGI218V (Production Commercial Copper)	926894	SLK3D	Tray
WGI219LM (Production Commercial Copper)	936393	Q REF	Tray
WGI219LM (Production Commercial Copper)	936396	SLKJ2	Tape & Reel
WGI219LM (Production Commercial Copper)	936399	SLKJ3	Tray
WGI219V (Production Commercial Copper)	936400	SLKJ4	Tape & Reel
WGI219V (Production Commercial Copper)	936401	SLKJ5	Tray

1.3 I218/I219 Production Marking Diagrams

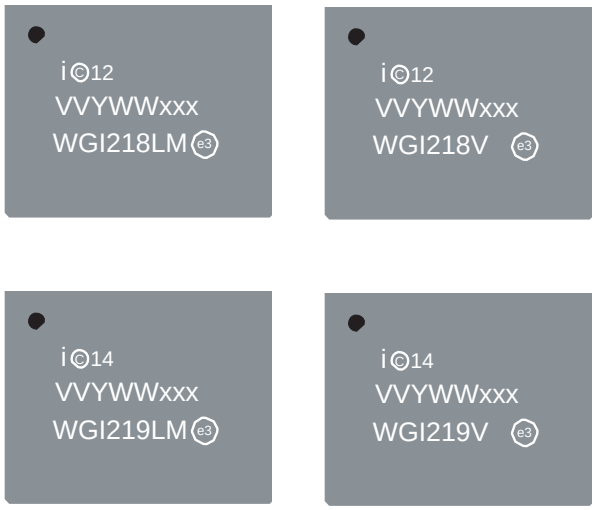

Figure 1-1 I218/I219 Production Top Marking Examples

Notes:

Line 1: Intel copyright with date code
Line 2: Fab Lot Trace Code - VVYWWxxx where VV=Assembly location code, Y=year indicator (R=2014, S=2015, etc.), WW=Work Week, and xxx= Batch identifier
Line 3: Product Code and Pb-free mark (e3 or e1)

1.4 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata and/or clarifications that apply to silicon/steppings. See Table 1-5 for a description.

Table 1-4 Terms, Codes & Abbreviations

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Name	Description
Yes or No	If the errata applies to a stepping, “Yes” is indicated for the stepping (for example: “A0=Yes” indicates errata applies to stepping A0). If the errata does not apply to stepping, “No” is indicated (for example: “A0=No” indicates the errata does not apply to stepping A0).
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Red Change Bar / or Bold	This Item is either new or modified from the previous version of the document.
DS	Data Sheet
DG	Design Guide
SDM	Software Developer’s Manual
EDS	External Data Specification
AP	Application Note

1.5 Hardware Sightings, Clarifications, Changes, Updates and Errata

See Section 1.4 for an explanation of terms, codes, and abbreviations.

Table 1-5 Summary of Hardware Clarifications, Changes and Errata; Errata Include Steppings

Specification Changes	Status
None.	N/A
Specification Clarifications	**Status**
1. Expected Link Down Behavior	N/A
Documentation Updates	**Status**
None	
Errata	**Status**
1. 10BASE-T TP_IDLE Mask Failure	B1 NoFix
2. 1000BASE-T Distortion (IEEE 2008 Spec Limitation)	B1 NoFix
3. Performance Degradation is Possible with Streams of 9KB Jumbo Frame Packets	B1 NoFix
4. FLR Mechanism Not Supported	B1 NoFix
5. Buffer Overrun While the I219 is Processing DMA Transactions	Intel® 100/200 Series Chipsets – NoFix Intel® 300 Series Chipsets - Fixed

1.5.1 Specification Changes

None at this time.

1.5.2 Specification Clarifications

1. Expected Link Down Behavior

When a network cable is removed from an active system, the link LED remains lit about two to five seconds. This is expected behavior for a link down.

1.5.3 Documentation Changes

None at this time.

1.5.4 Errata

1. 10BASE-T TP_IDLE Mask Failure

Problem:

The 10BASE-T link pulse wave form touches the template mask due to a small voltage glitch when switching from active to low-power mode. Some designs might have a mask failure on the 10BASE-T (1411.10.06) TP_IDLE, both with and without the TPM (Twisted Pair Model).

Implication:

No implication on system level performance or interoperability. The IEEE conformance test is the only impact.

Workaround:

None.

Status:

B1 NoFix

2. 1000BASE-T Distortion (IEEE 2008 Spec Limitation)

Problem:

1000BASE-T IEEE 2008 distortion specification (40.6.1.2.4); a PHY is considered to pass this test if the peak distortion is below 10mV for at least 60% of the UI within the eye opening. The I218 Gigabit Ethernet Controller may marginally fail this requirement at the HTLV corner. At nominal operating conditions using the latest NVM (version 1.2 or later), the I218 will pass.

Implication:

No implication on system level performance or interoperability. The only impact is the IEEE test conformance.

Workaround:

None.

Status:

B1 NoFix

3. Performance Degradation is Possible with Streams of 9KB Jumbo Frame Packets

Problem:

When a platform sends a long burst of back-to-back jumbo frames (size is 9 KB) and the Inter-Packet Gap (IPG) is minimal, the performance can be degraded with up to 1/2500 packets lost.

Implication:

The system experiences performance degradation when using 9 KB jumbo frames sent back-to-back with a minimal IPG.

Workaround:

None.

Note: Reducing the MTU/maximum jumbo frame size to 8.5 KB eliminates the possibility of performance degradation.

Status:

B1 NoFix

4. FLR Mechanism Not Supported

Problem:

The Media Access Controller (MAC) in PCH advertises by default a Function Level Reset (FLR)/ Advanced Function Level Reset (AFLR) capability in their PCI configuration space. However, the FLR mechanism is not supported by these devices.

Implication:

Using the FLR/AFLR mechanism can cause network adapter hang and in some cases can lead to system instability.

When FLR/ AFLR is triggered, the system might lose synchronization between the integrated MAC and the external Physical Layer (I219LM/ I219V PHY), from which it cannot recover.

Workaround:

Using the PMCSR register to perform D0->D3->D0 transition or using the MMIO register CTRL.SWRST might be considered as an alternative, depending on the required reset level.

Status:

B1 NoFix

5. Buffer Overrun While the I219 is Processing DMA Transactions

Problem:

Intel® 100/200 Series Chipset platforms reduced the round-trip latency for the LAN Controller DMA accesses, causing in some high-performance cases a buffer overrun while the I219 LAN Connected Device is processing the DMA transactions.

Implication:

I219LM and I219V devices can fall into unrecovered Tx hang under very stressfully UDP traffic and multiple reconnection of Ethernet cable. This Tx hang of the LAN Controller is only recovered if the system is rebooted.

Workaround:

Slightly slow down DMA access by reducing the number of outstanding requests. This workaround could have an impact on TCP traffic performance and could reduce performance up to 5 to 15% (depending) on the platform. Disabling TSO eliminates performance loss for TCP traffic without a noticeable impact on CPU performance.

Status:

Intel® 100/200 Series Chipsets – NoFix
Intel® 300 Series Chipsets - Fixed

2. Software Clarifications

Table 1-1 Summary or Software Clarifications

Software Clarifications	Status
None.	N/A