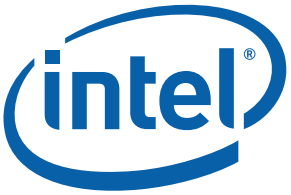

Intel® Ethernet Controller I217 Specification Update

February 2013
Revision 1.0

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Revision History

Date	Revision	Description
February 2013	1.0	Initial Release (Intel Public).

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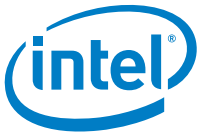

1.1 Introduction and Scope

This document applies to the Intel® Ethernet Controller I217.

This document is an update to a published specification, the *Intel® Ethernet Controller I217 Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.2 Product Code and Device Identification

Product Codes: WGI217LM and WGI217V (Commercial Copper).

The following tables and component drawings describe the various identifying markings on each device package:

Table 1-1 Markings

Device	Stepping	Top Marking	Description
I217LM	A3	WGI217LM	Production Commercial Copper
I217V	A3	WGI217V	Production Commercial Copper

Table 1-2 Device IDs

I217 Device ID Code	Vendor ID	Device ID
I217LM	0x8086	0x153A
I217V	0x8086	0x153B

Table 1-3 MM Numbers

Product	MM Number	Specification Code	Media
WGI217LM (Production Commercial Copper)	924105	SLJWE	Tape and Reel
WGI217LM (Production Commercial Copper)	924107	SLJWF	Tray
WGI217V (Production Commercial Copper)	924196	SLJWG	Tape and Reel
WGI217V (Production Commercial Copper)	927464	SLJWH	Tray

1.3 I217 Production Marking Diagrams

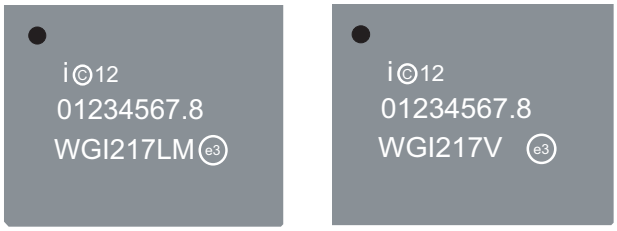

Figure 1-1 I217 Production Top Marking Examples

Notes:

Line 1: With no spaces, “i”©YY
Line 2: Fab Lot Trace Code 0123456.78 (10-char max)
Line 3: S-Spec Code and Pb-free mark (e3 or e1)

1.4 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata and/or clarifications that apply to silicon/steppings. See Table 1-5 for a description.

Table 1-4 Terms, Codes, Abbreviations

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification’s impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Yes or No	If the errata applies to a stepping, “Yes” is indicated for the stepping (for example: “A0=Yes” indicates errata applies to stepping A0). If the errata does not apply to stepping, “No” is indicated (for example: “A0=No” indicates the errata does not apply to stepping A0).
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

Name	Description
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Red Change Bar / or Bold	This Item is either new or modified from the previous version of the document.
DS	Data Sheet
DG	Design Guide
SDM	Software Developer's Manual
EDS	External Data Specification
AP	Application Note

1.5 Hardware Sightings, Clarifications, Changes, Updates and Errata

See Section 1.4 for an explanation of terms, codes, and abbreviations.

Table 1-5 Summary of Hardware Clarifications, Changes and Errata; Errata Include Steppings

Specification Changes	Status
None.	N/A
Specification Clarifications	**Status**
None	N/A
Documentation Updates	**Status**
None	
Errata	**Status**
1. 10BASE-T TP_IDLE Mask Failure	A3 NoFix
2. 1000BASE-T Distortion (IEEE 2008 Spec Limitation)	A3 NoFix

1.5.1 Specification Changes

None at this time.

1.5.2 Specification Clarifications

None at this time.

1.5.3 Documentation Changes

None at this time.

1.5.4 Errata

1. 10BASE-T TP_IDLE Mask Failure

Problem:

The 10BASE-T link pulse wave form touches the template mask due to a small voltage glitch when switching from active to low-power mode. Some designs might have a mask failure on the 10BASE-T (1411.10.06) TP_IDLE, both with and without the TPM (Twisted Pair Model).

Implication:

No implication on system level performance or interoperability. The IEEE conformance test is the only impact.

Workaround:

None.

Status:

A3 NoFix

2. 1000BASE-T Distortion (IEEE 2008 Spec Limitation)

Problem:

1000BASE-T IEEE 2008 distortion specification (40.6.1.2.4); a PHY is considered to pass this test if the peak distortion is below 10mV for at least 60% of the UI within the eye opening. The I217 Gigabit Ethernet Controller may marginally fail this requirement at the HTLV corner. At nominal operating conditions using the latest NVM (version 1.2 or later), the I217 will pass.

Implication:

No implication on system level performance or interoperability. The only impact is the IEEE test conformance.

Workaround:

None.

Status:

A3 NoFix

2. Software Clarifications

Table 1-1 Summary or Software Clarifications

Software Clarifications	Status
None.	N/A