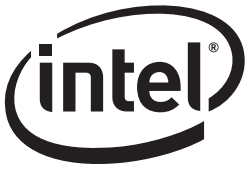

82541ER Gigabit Ethernet Controller
Specification Update

January 2011

The *82541ER* Gigabit Ethernet Controller may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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REVISION HISTORY

Date of Revision	Description
January 2011	Revised sections “Component Identification via Programming Interface” and “General Information”.
November 2009	Added errata #6 through #9. Added specification clarification #2.
July 2005	Changed revision number in the Component Identification via Programming Interface table from 00h to 05h.
March 2005	Removed Errata #4, 5, 6 – not applicable to 82541ER.
February 2005	Added erratum number 8, “82541ER Gigabit Ethernet Controller Might Fail to Wake Up a System. Added C-0 stepping information.
April 2004	Included Specification Change 1, “General Operating Conditions for 1.8V and 1.2V.” Added erratum number 7, “Possible Ripple on 1.8V and 1.2V Regulator Outputs.” Added Specification Clarification 1, “Oscillator Support.”
October 2003	Initial non-classified release.

PREFACE

This document is an update to published specifications. Specification documents for these products include:

- 82541ER Gigabit Ethernet Controller Datasheet.
- 82541PI/GI/EI, 82541ER, & 82547GI(EI) EEPROM Map and Programming Information Guide, Intel Corporation.
- 82541ER Design Guide

For software driver programming information, contact your Intel representative.

This document is intended for hardware system manufactures and software developers of applications, operating systems or tools. It may contain Specification Changes, Errata, and Specification Clarifications.

All 82541ER product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

NOMENCLATURE

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

COMPONENT IDENTIFICATION VIA PROGRAMMING INTERFACE

82541ER controller steppings are identified by the following register contents:

Stepping	Vendor ID	Device ID	Revision Number
82541ER C-0	8086h	1078h	05h

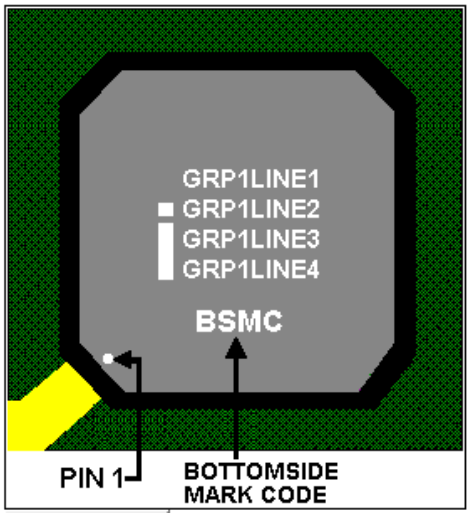
These devices also provide identification data through the Test Access Port.

GENERAL INFORMATION

This section covers the 82541ER devices.

82541ER COMPONENT MARKING INFORMATION

Product	Stepping	Top Marking	Notes
82541ER	C-0	82541ER	Production Units



SUMMARY TABLE OF CHANGES

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82541ER steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLES

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

No.	C0	Plans	SPECIFICATION CHANGES	Page	Notes
1	X	NoFix	General Operating Conditions for 1.8V and 1.2V	8	-
No.	**C0**	**Plans**	**ERRATA**	**Page**	**Notes**
1	X	NoFix	Master-Aborts with Some Chipsets During Driver-Initiated Controller Reset	8	-
2	X	NoFix	Marginal Internal Power on Reset Function	9	-
3	X	NoFix	Full Duplex Partner Assumed when Shifting from 1000BASE-T to 100BASE-TX	9	-
4	X	NoFix	Possible Ripple on 1.8V and 1.2V Regulator Outputs	9	-
5	X	Fix	82541ER Gigabit Ethernet Controller Might Fail to Wake Up a System	10	-
6	X	NoFix	Receive Packet Delayed When Using RDTR or RADV Register	10	
7	X	NoFix	MNG: Pass-Through From BMC to LAN Hangs During PCI Reset	10	
8	X	NoFix	MNG:SMBus Hang When Delay Between Transactions is Less Than 10 µs	10	
9	X	NoFix	Overwrites Transmit Descriptors in Internal Buffer	11	
No.	**C0**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Page**	**Notes**
1	X		External Oscillator Support	11	-
2	X		82541ER Software Device Drivers in Release 14.7 Are the Final WHQL Drivers	11	-

SPECIFICATION CHANGES

1. General Operating Conditions for 1.8V and 1.2V

Problem: This change is related to erratum 4, “Possible Ripple on 1.8V and 1.2V Regulator Outputs,” listed in this document. Due to this anomaly, the following specifications were modified to the following:

Symbol	Parameter	Min	Max	Units
Vdd (1.8)	DC supply Voltage on 1.8V pins	1.71	1.89	V
Vdd (1.2)	DC supply Voltage on 1.2V pins	1.14	1.26	V
Voltage Ramps				
1.8V Ripple	Maximum voltage ripple at frequency below 1 MHz		280	mV peak-to-peak
1.8V Ripple	Maximum voltage ripple at frequency below 1 MHz **Note:** This is the lowest absolute voltage for the frequency range below 1 MHz.	1.55		V
1.2V Ripple	Maximum voltage ripple at frequency below 1 MHz		180	mV peak-to-peak
1.2V Ripple	Maximum voltage ripple at frequency below 1 MHz **Note:** This is the lowest absolute voltage for the frequency range below 1 MHz.	1		V

ERRATA

1. Master-Aborts with Some Chipsets during Driver-Initiated Controller Reset

Problem: The 82541ER Gigabit Ethernet Controller implements a software-Initiated device reset function through the control register space (Control Register, bit 26). This software-initiated reset re-initializes all functional states of the controller except for PCI/PCI-X configuration. When the reset is written, the controller requires a few internal clock cycles to complete the reset operation. During this brief time, they will not respond to additional register accesses.

Some PCI/PCI-X bridge components implemented with internal 64-bit architectures may initiate an additional zero byte write immediately following a 32-bit write to the device CTRL register. This zero byte write is essentially padding for a 64-bit transaction. In cases where the CTRL register access performs a software reset of the controller, the zero byte operation may encounter a master abort due to the controller reset in progress.

Implication: In most system configurations, a master abort on an outbound 0-byte write operation will not result in any adverse system behavior. However, the event may be logged at the chipset, bridge, or operating system level.

If the bridge/chipset is configured to promote the master abort to a Non-Maskable Interrupt (NMI) and the operating system cannot discern and handle NMI events, then a fatal operating system error may occur.

Workaround: The 82541ER device can only be accessed using DWord (32-bit) software operations. Since the potential zero byte write immediately following a device CTRL register write is a hardware event created by the chipset bridge components, no software mechanism can be used to eliminate the 0-byte write operation.

When an operating system is incapable of handling the NMI event, the chipset or bridge should be configured to avoid promoting this master abort to a fatal NMI event. Alternatively, the software-initiated device reset may be performed using an I/O access in place of a memory-mapped device access. The latter solution is effective if master aborts on I/O writes do not result in NMI.

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

2. Marginal Internal Power on Reset Function

Problem: Power on (internal) Reset is not dependable in the event of a slow power ramp. If the 3.3V supply ramps slowly, the 1.2V supply (from the collector of the external PNP pass transistor) may not be stable when reset occurs. Voltage thresholds are not within design targets.

Implication: Internal power on reset is an alternative to using the LAN_PWR_GOOD input. To enable power on reset, LAN_PWR_GOOD must be connected to 3.3V through a pull-up resistor. For this configuration, a power ramp specification must be imposed and the 3.3V supply ramps from its 10% point to its 90% point in less than 15 ms. This requirement is more restrictive than the general recommendation that all power supplies should ramp to within their regulation bands in less than 20 ms.

Workaround: The LAN_PWR_GOOD signal should be connected to the system's voltage supervisor function. Using LAN_PWR_GOOD as the external reset input is the preferred method.

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

3. Full Duplex Partner Assumed when Shifting from 1000BASE-T to 100BASE-TX

Problem: For a link partner that advertises 1000BASE-T full duplex and 100BASE-TX half duplex capabilities, the 82541ER will attempt to link at 1000 Mbps, followed by 100 Mbps. However, it will assume the link partner is capable of full duplex operation at both speeds.

Implication: If the advertisement is correct, a problem could occur obtaining link. By default, practical Gigabit Ethernet devices are capable of full duplex operation at both 1000 Mbps and 100 Mbps. Thus, the possibility of this advertisement is very low.

Workaround: There is no workaround for this erratum.

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

4. Possible Ripple on 1.8V and 1.2V Regulator Outputs

Problem: The internal ground bounce that occurs when the 82541ER drives the PCI bus can introduce ripple on the 1.2V and 1.8V linear voltage regulator (LVR) outputs. This ripple violates the published DC specification (nominal voltage of –7% and +5%).

Implication: The ripple of concern occurs at a frequency below 1 MHz. When these voltage levels are measured, higher frequency noise components will be seen super-imposed on the lower frequency (less than 1 MHz) ripple. These higher frequency glitches are unrelated to the LVR functionality and should be disregarded. When measuring this ripple, it is recommended that the scope bandwidth is limited to the greatest extent to filter out noise greater than 1 MHz.

Under normal network data conditions (random data patterns); this ripple does not violate the current DC specification values. However, under heavy simultaneous switching loads presented over prolonged periods of time (such as sequential large packets with worst case data transition patterns received over the network), the ripple can violate the specified DC values. Worst case data patterns are those that cause the majority of 32 PCI data outputs to simultaneously switch from one to zero in a repeated pattern, such as FFFF FFFFh, 0000 0000h, FFFF FFFFh, 0000 0000h, etc.

Note: There have been no customer reports related to this ripple component. The specification violation has only been observed during testing using a SmartBits network exerciser to generate sustained worse case loads.

The 82541ER can tolerate a periodic voltage variation beyond the existing DC specification to a degree specified in a revised DC and new AC ripple specification without impact to device functionality or reliability. If the ripple component exceeds the value of the new AC specification, decreased BER performance may result. The Ethernet link may also be reset, causing link to be lost and re-established.

Root Cause: Extreme switching (for example, sequences of sequential packets with worst case pattern type data) of the PCI data output buffers causes internal switching currents that disrupt the LVR reference voltage.

Workaround: There is no workaround for this switching noise when an internal LVR is used. If external voltage regulators are used, switching noise will not occur since the external regulators are not affected by the internal ground bounce on the LVR.

Status: The updated specifications are listed in the Specification Changes section of this document.

5. 82541ER Gigabit Ethernet Controller Might Fail to Wake Up a System

Problem: An 82541ER Gigabit Ethernet controller might fail to wake up a system upon receiving a “magic” packet.

Implication: Under extreme circumstances (approximately 1,500 to 2,000 continuous boots), an 82541ER Ethernet controller might fail to wake up a system upon receiving and correctly identifying a magic packet from a LINK partner.

Workaround: Always send a second packet to wake the system up. If the first magic packet fails to wake up the system, then a second packet always succeeds. If the first magic packet wakes up the system, then hardware simply ignores the second packet.

Status: Intel does not plan to resolve this erratum in the 82546GB Gigabit Ethernet Controller.

6. Receive Packet Delayed When Using RDTR or RADV Register

Problem: When using the RDTR and/or RADV timer mechanisms, there could be a situation where the write-back timer is incorrectly disabled, which prevents the write-back of a receive descriptor until another packet arrive.

Implication: No packet loss will occur. There may however, be a large delay between the time an Rx packet is received in the device and the time the descriptor is written back to memory, and finally an interrupt generated.

Workaround: It is recommended that the RDTR and RADV registers not be used for moderating Rx interrupts. The preferred solution is to use the Interrupt Throttling Register; ITR.

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

7. MNG: Pass-Through From BMC to LAN Hangs During PCI Reset

Problem: When a PCI reset occurs while a packet is being passed through from the BMC to the LAN, the FIFO control logic may hang.

Implication: BMC can no longer transmit to the LAN.

Workaround: Contact your Intel representative for the latest NVM release which includes an SMBus command that allows the BMC to reset the manageability logic. The BMC should send this command when a hang is detected.

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

8. MNG: SMBus Hang When Delay Between Transactions is Less Than 10 µs

Problem: When the time between the STOP and START is less than 10 µs, the SMBus logic may hang. This appears externally as a clock stretch which hangs the SMBus. The standard requires a minimum of 4 us between STOP and START.

Implication: No SMBus communication.

Workaround: Contact your Intel representative for the latest NVM release.

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

9. Overwrites Transmit Descriptors in Internal Buffer

Problem: This erratum occurs when the internal transmit descriptor buffer is nearly full of descriptors. If the free space in this buffer is smaller than the system cacheline, the calculation of the size of the descriptor fetch may be incorrect.

Implication: Corruption of the transmit descriptor ring; can cause a system crash. In most applications, the descriptors will be written back as soon as the data has been read and they will not be accumulating in the internal buffer, therefore this issue will not be seen. However, in an application where system events prevent the immediate write-back of descriptors, the descriptor buffer could fill up and this issue could be seen.

Workaround: The driver should keep track of the difference between the Transmit head and tail and make sure the difference between tail and head is never more than the value shown below:

Cacheline	Maximum Value (TDT-TDH)
32 bytes	62
64 bytes	60
128 bytes	56
256 bytes	48

Status: Intel does not plan to resolve this erratum in the 82541ER Gigabit Ethernet Controller.

SPECIFICATION CLARIFICATIONS

1. External Oscillator Support

Clarification: The 82541ER clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used in place of the crystal with the proper design considerations:

- The clock oscillator has an internal voltage regulator of 1.2 V to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude of 1.2 V.
- The input capacitance introduced by the 82541ER (approximately 20 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the 82541ER clock and its performance.

2. 82541ER Software Device Drivers in Release 14.7 Are the Final WHQL Drivers

Clarification: Any changes to the current 82541ER Windows software device driver will no longer be WHQLd. Windows 7 and Windows 2008 Server R2 will only provide in-box base driver support. There will be no support for any future Windows operating systems.

Note that Linux kernel 2.6.31 is the last kernel that is validated for the 82541ER.

DOCUMENTATION CHANGES

No documentation changes reported at this time.